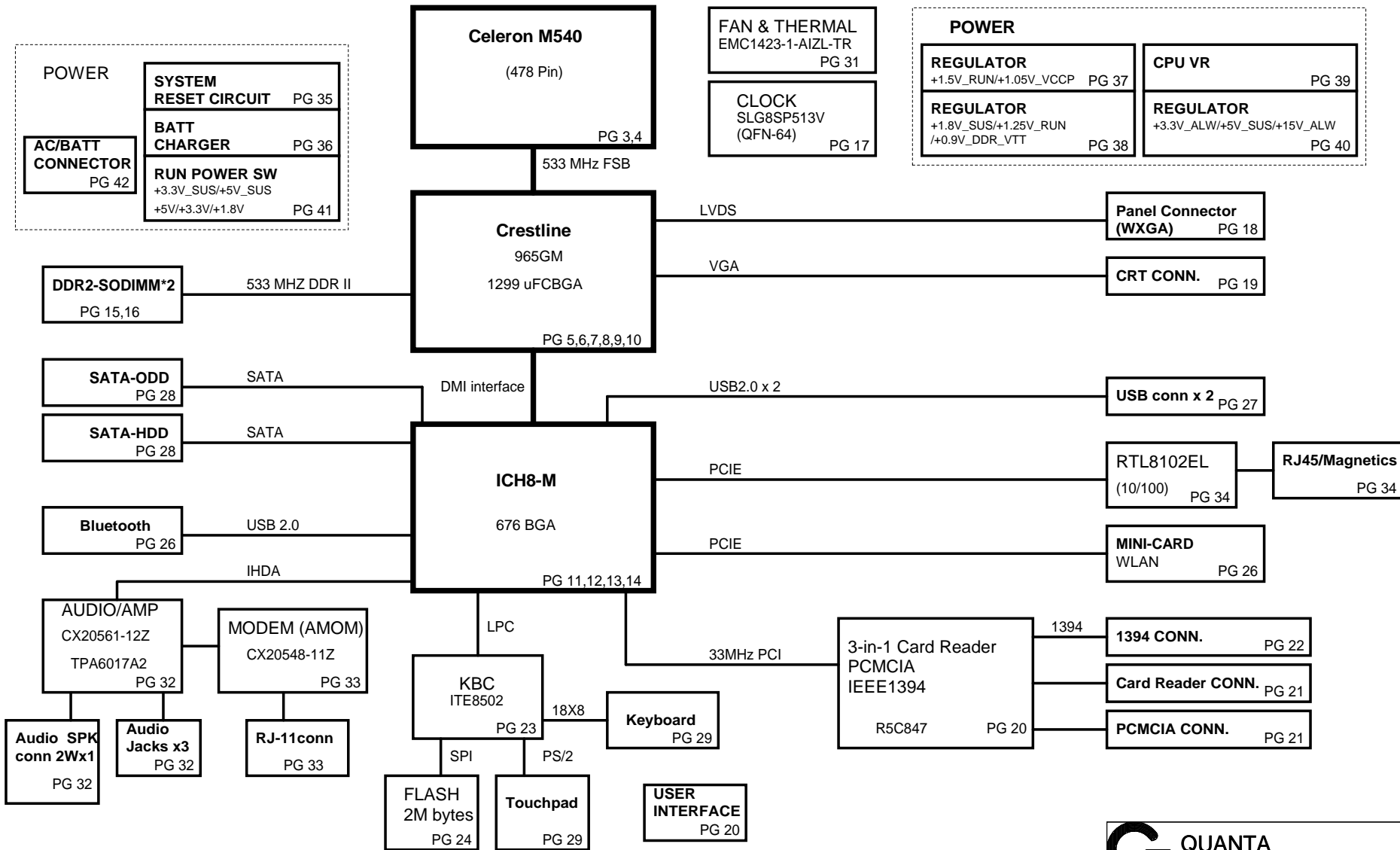


VM9/VM8 Block Diagram

VER : 1A



Title		
Schematic Block Diagram		
Size	Document Number	Rev
	VM9/VM8	1A
Date:	Friday, July 18, 2008	Sheet 1 of 53


Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Merom
5-10	Crestline
11-14	ICH8M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18	HDMI
23	LCD Conn. & SSP
24	CRT Conn
25	SATA Conn
26-27	CARD READER/Conn & 1394
28	Express Card & Smart Card
29-30	Mini Card
31	SIO (ITE8512)
32	FLASH/RTC
33	USB
35	TP / KEYBOARD
36	SWITCH /LED
37	FAN & Thermal
38-39	Audio CODEC(ALC888)/Phone Jack
40-41	LOM / Switch
44	System Reset Circuit
46	Battery Selector & Charger
48	1.05VCCP / 1.5VRUJN
49	DDR2_1.8VSUS, 0.9V
51	CPU_ISL6266(2phase)
52	MAX8744 (+5.5V,+3.3V)
53	RUN Power Switch
54	DCIN,Batt
55	PAD& SCREW
56	EMI CAP
57	SMBUS BLOCK
58	Power Block Dianram

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,51,52,56	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54,56	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,26,30,37,38,43,48,49,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	18,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	

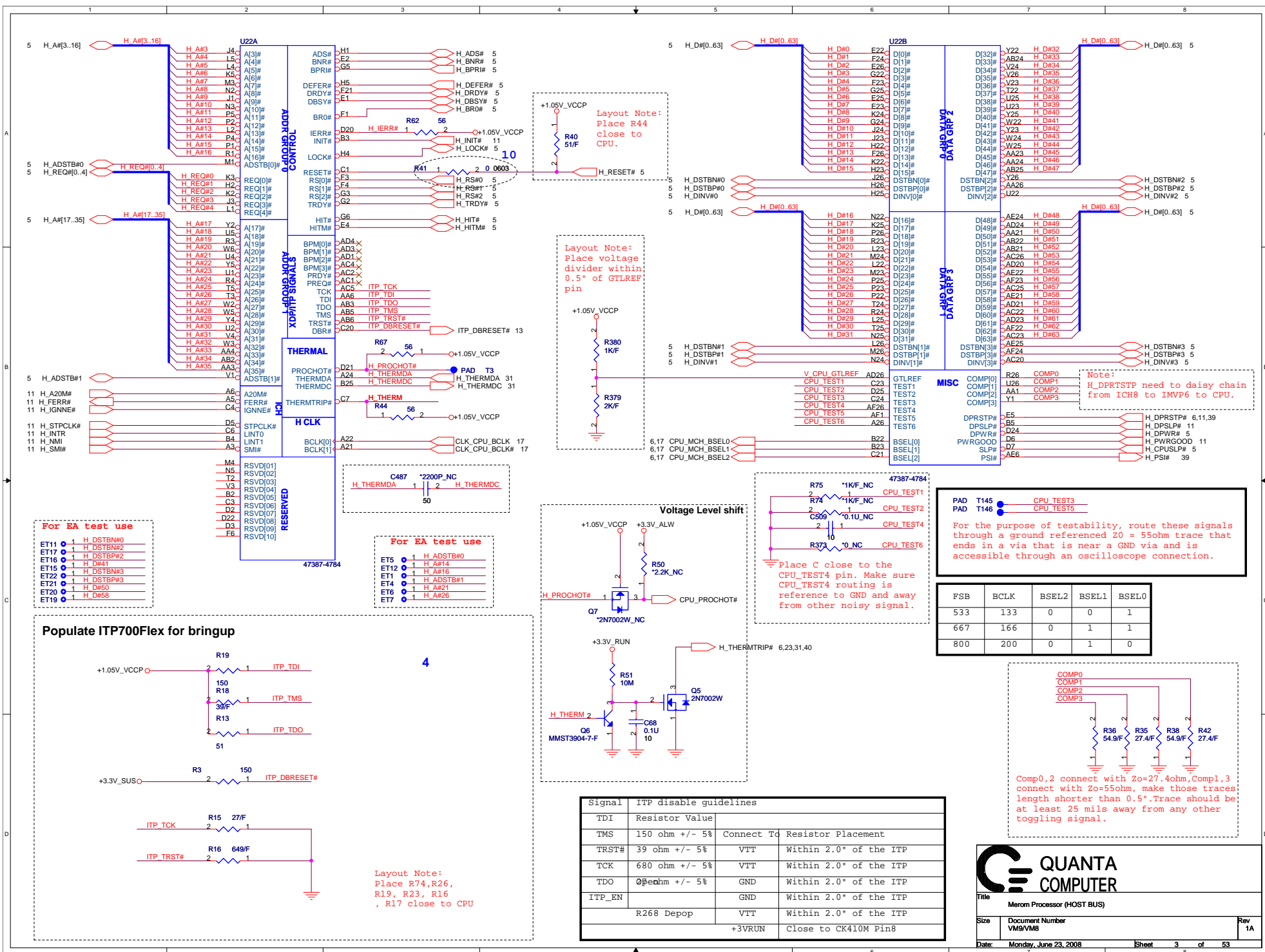
GND PLANE	PAGE	DESCRIPTION
⏏ 8731AGND	46	
⏏ AGND_0.9V	49	
⏏ AGND_DC/DC	52	
⏏ AGND_DC2	48	
⏏ AGND_DDR	49	
⏏ AGND_ISL6260	51	
⏏ GND	ALL	


**QUANTA
COMPUTER**

Title: Index & Power Status

Size: Document Number VM9/VM8 Rev 1A

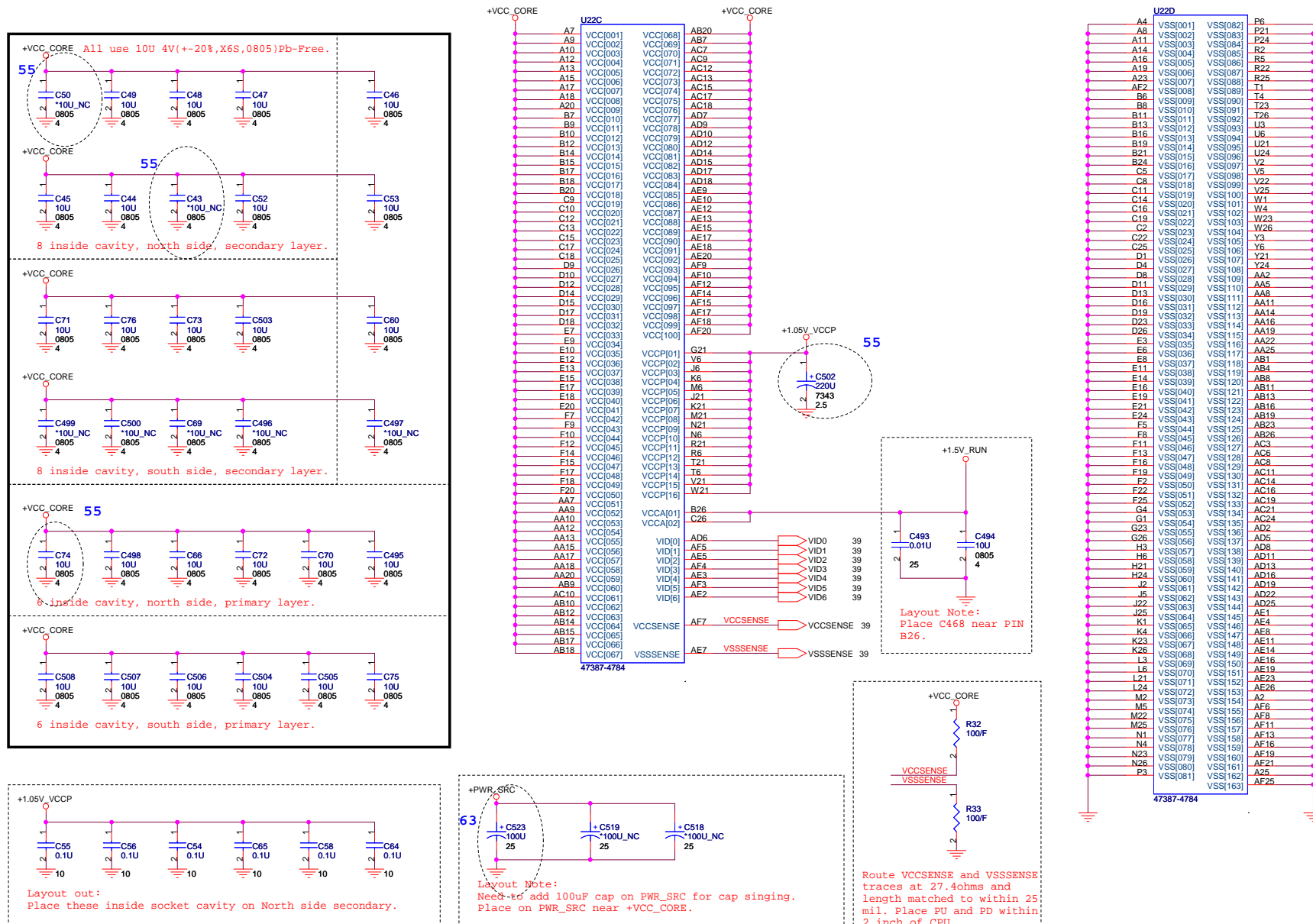
Date: Tuesday, May 27, 2008 Sheet 2 of 53



ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	0 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	0 ohm +/- 5%	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	GND	Within 2.0" of the ITP
		+3VRUN	Close to CK410M Pin8

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0





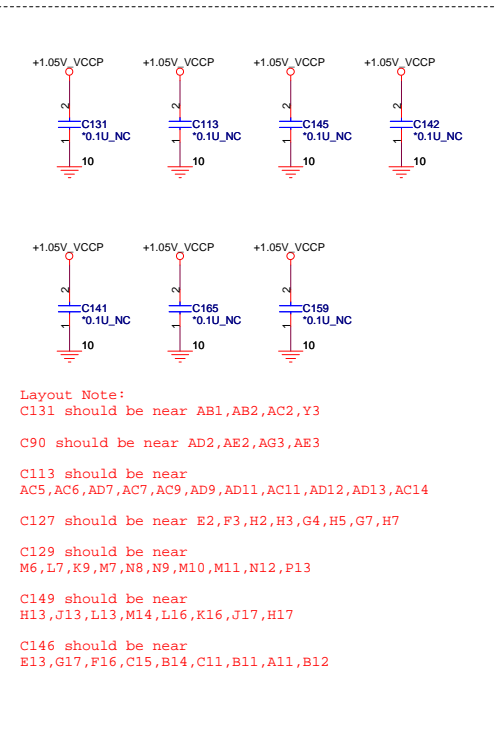
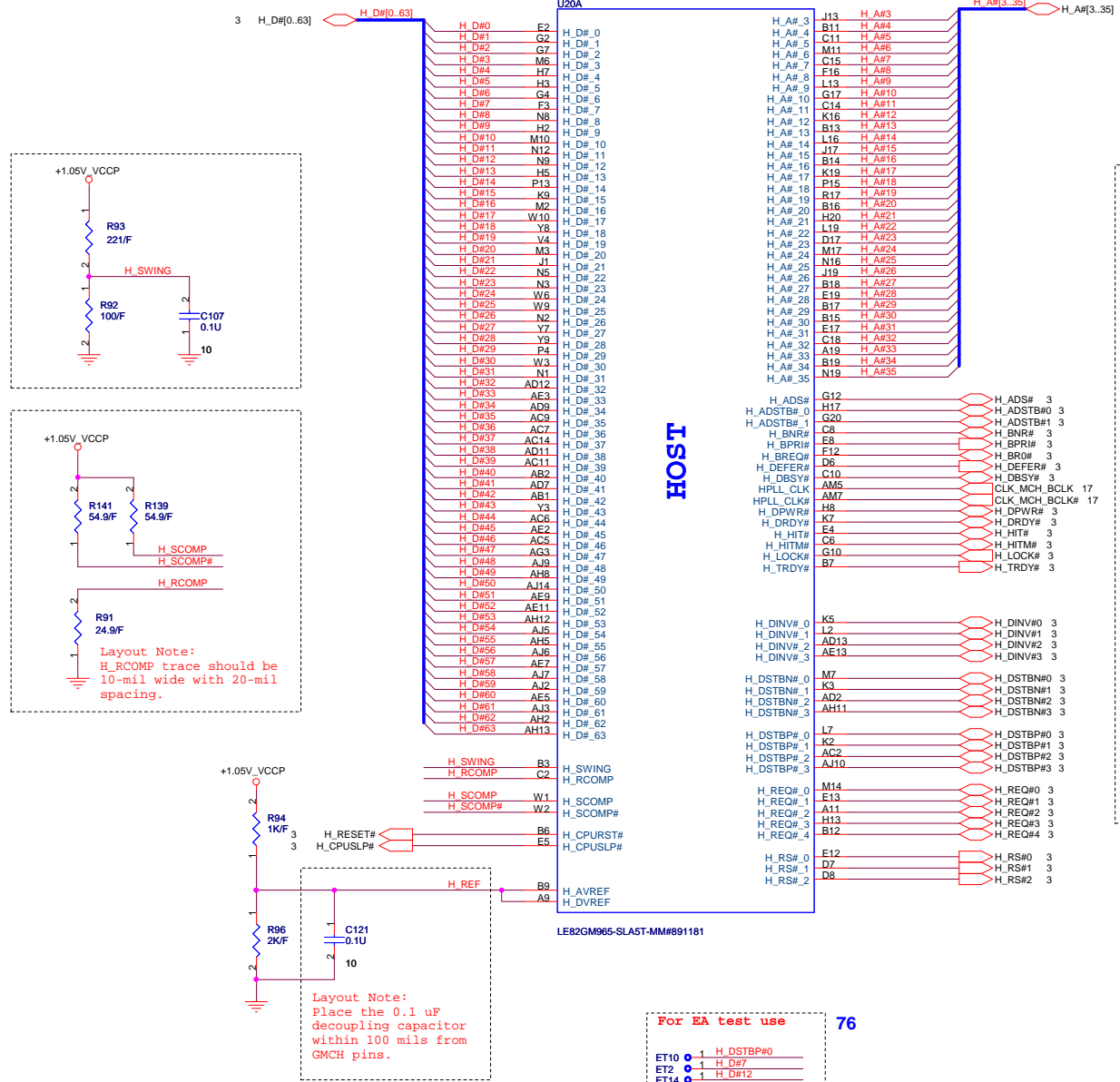
Title Merom Processor (POWER)

Size Document Number VM9/VM8

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Rev 1A



HOST

For EA test use

- ET10 1 H_DSTBP#0
- ET2 1 H_D#7
- ET14 1 H_DSTBN#1
- ET19 1 H_DSTBP#1
- ET18 1 H_D#29
- ET13 1 H_D#21
- ET3 1 H_D#21
- ET18 1 H_D#32



QUANTA
COMPUTER

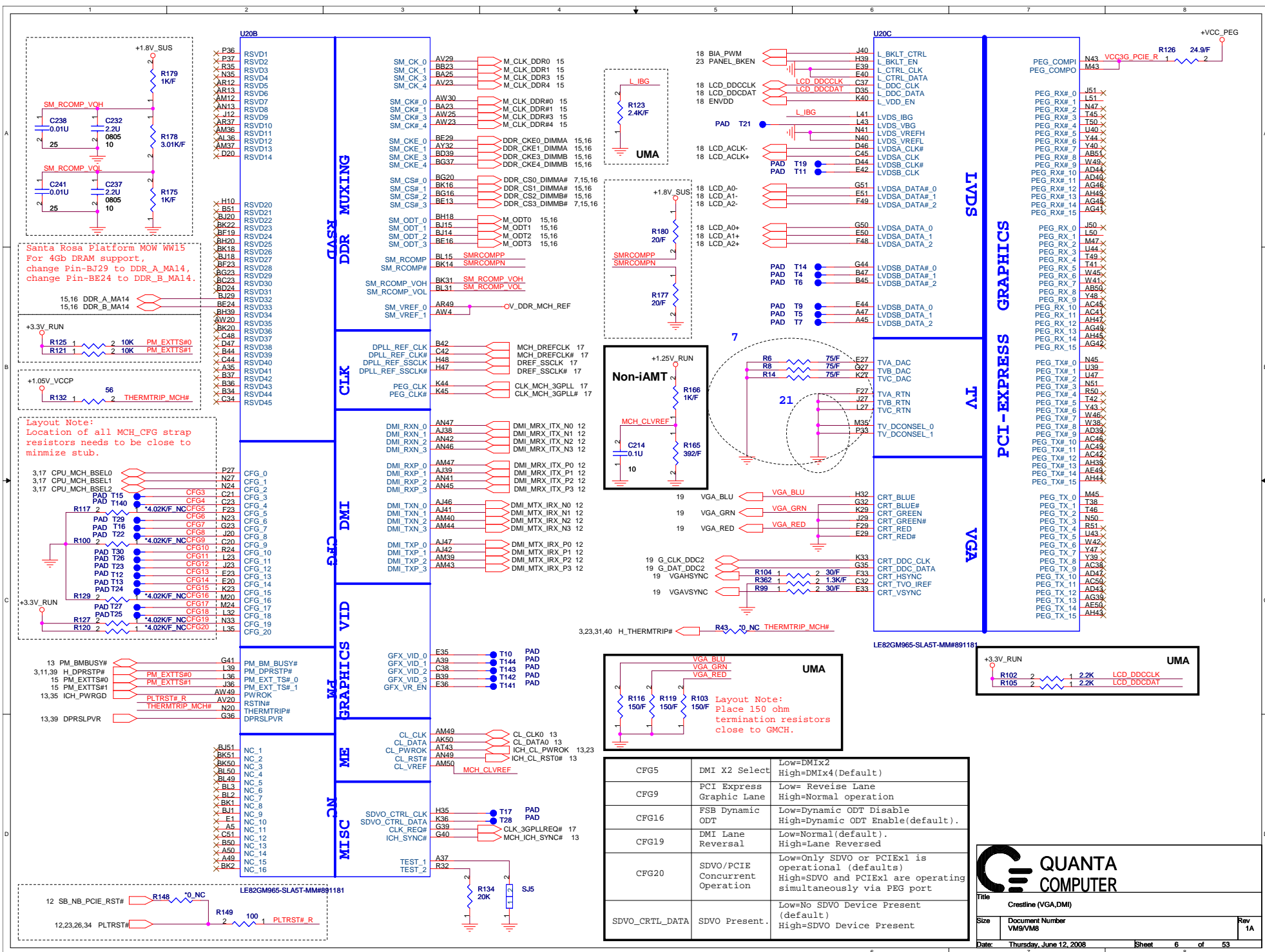
TitleCrestline (HOST)

SizeDocument NumberVM9/VM8

DateMonday, June 02, 2008

Rev1A

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Santa Rosa Platform MOW W15
For 4GB DRAM support,
change Pin-BJ29 to DDR_A_Ma14,
change Pin-BE24 to DDR_B_Ma14.

Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minimize stub.

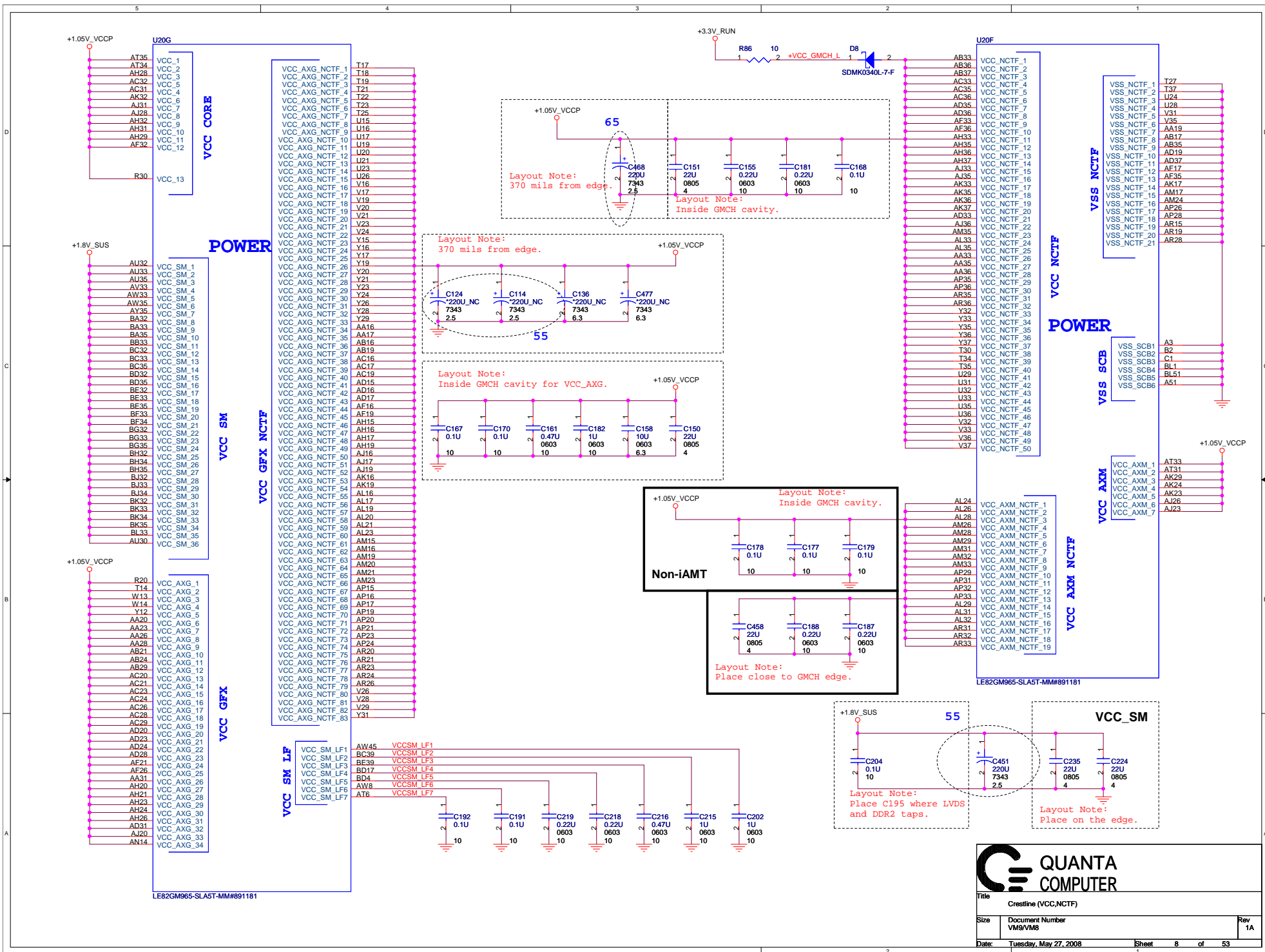
UMA
Layout Note:
place 150 ohm
termination resistors
close to GMCH.

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present..	Low=No SDVO Device Present (default) High=SDVO Device Present

**QUANTA
COMPUTER**

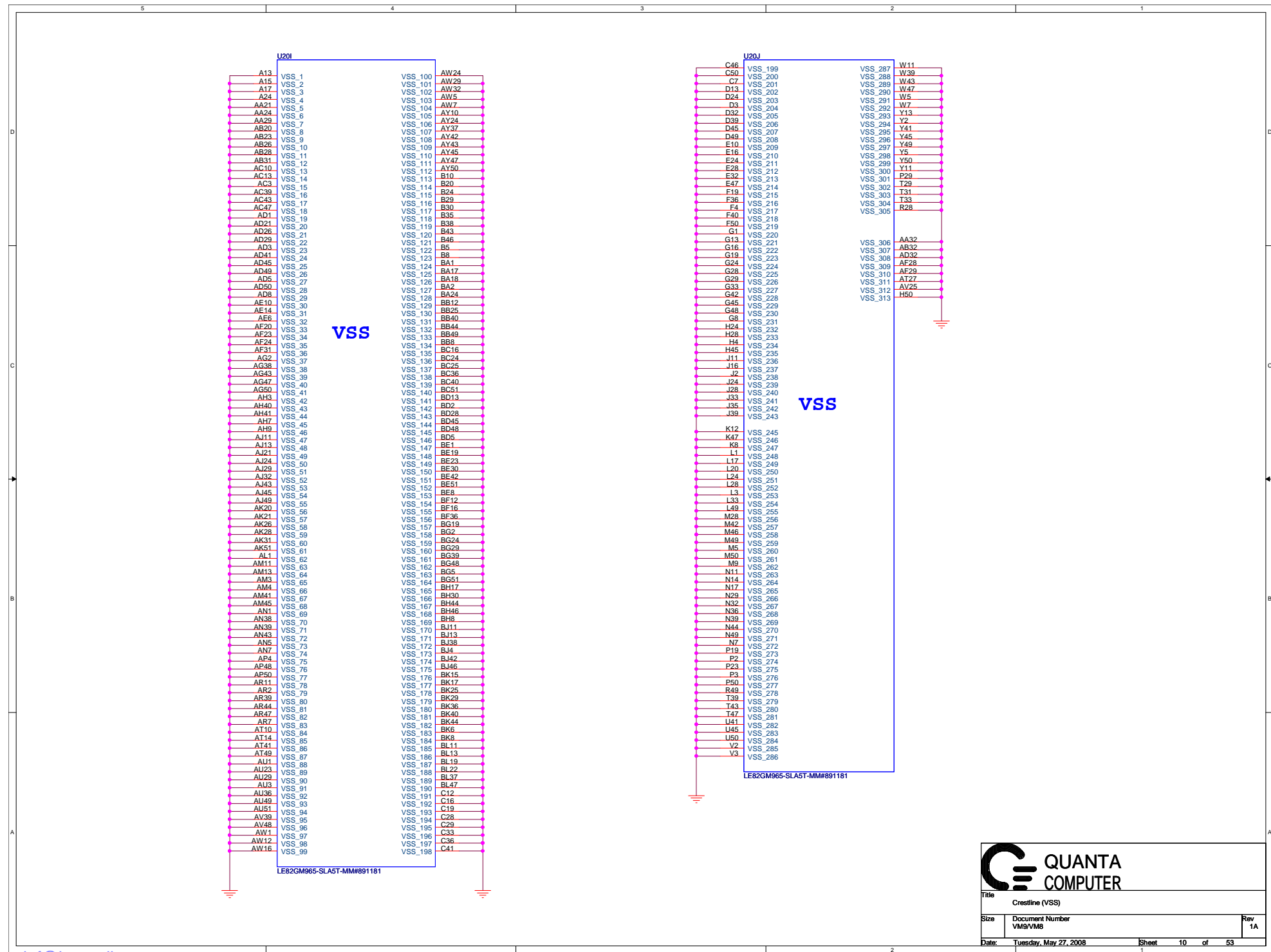
Title		Crestline (VGA,DMI)	
Size	Document Number	Rev	
	VM9/VM8	1A	
Date: Thursday, June 12, 2008		Sheet 6 of 53	





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COMPUTER

Title		Crestline (VCC,NCTF)	
Size	Document Number	Rev	
	VM9/VM8	1A	
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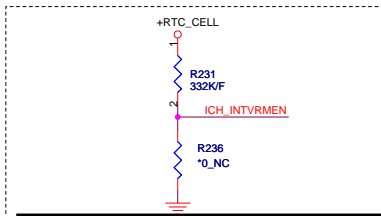
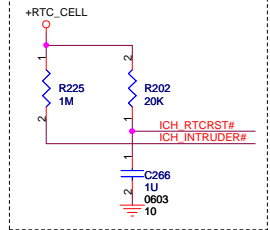
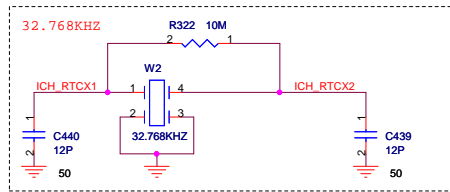
Title Crestline (VSS)

Size Document Number VM9/VM8

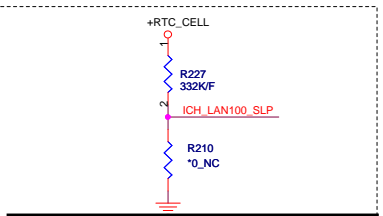
Rev 1A

Date: Tuesday, May 27, 2008

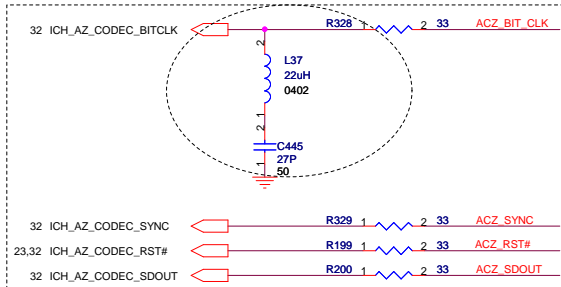
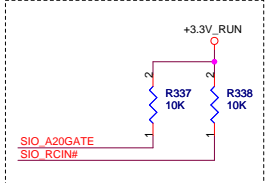
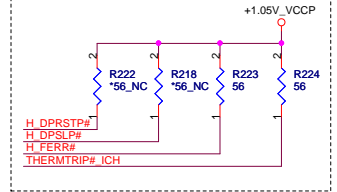
Sheet 10 of 53



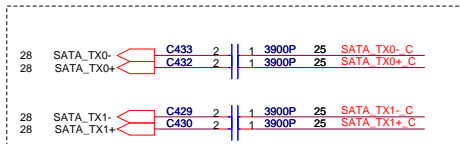
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)



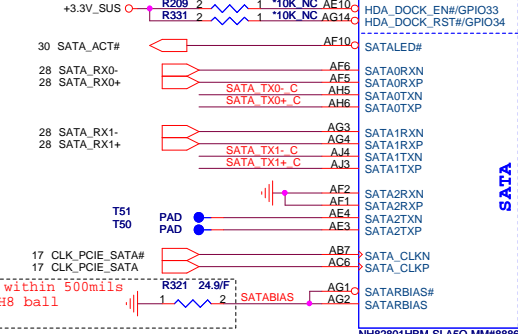
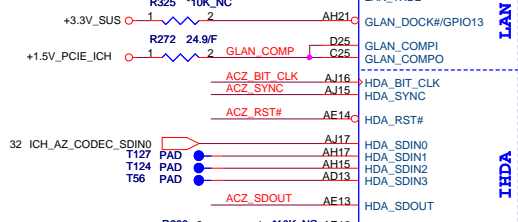
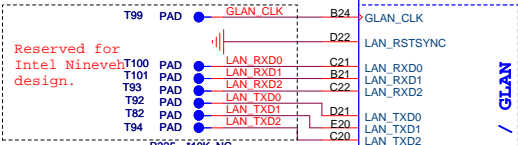
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



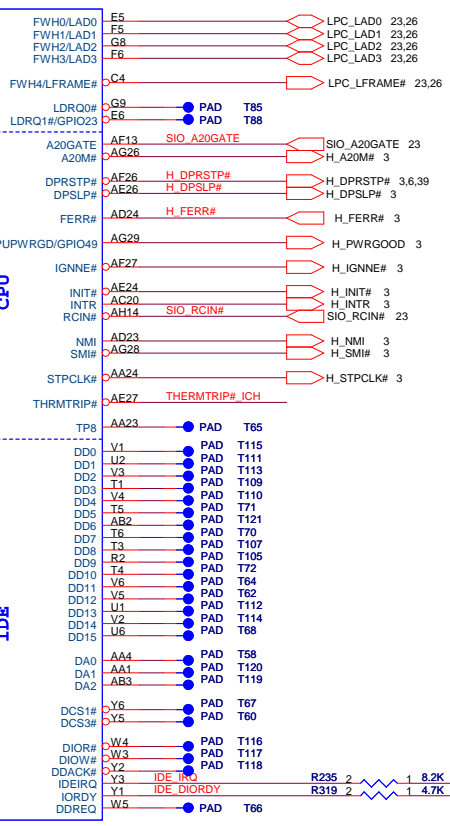
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source.



Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.



XOR Chain Entrance Strap		
ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1



**QUANTA
COMPUTER**

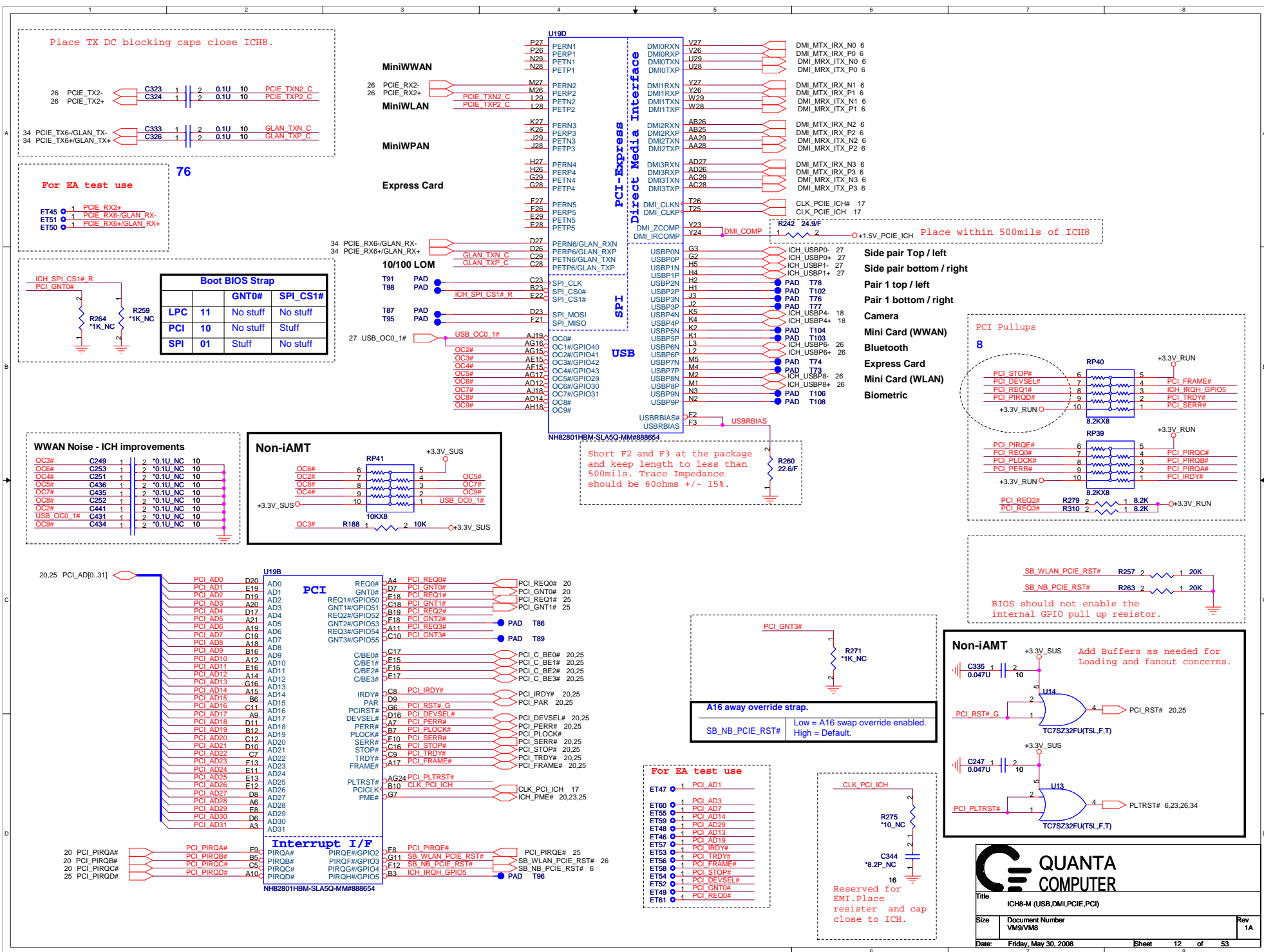
Title: ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)

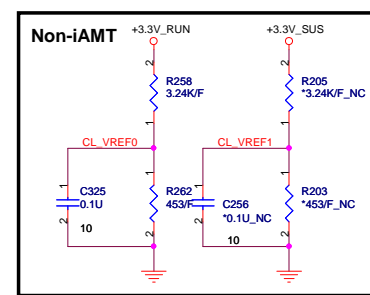
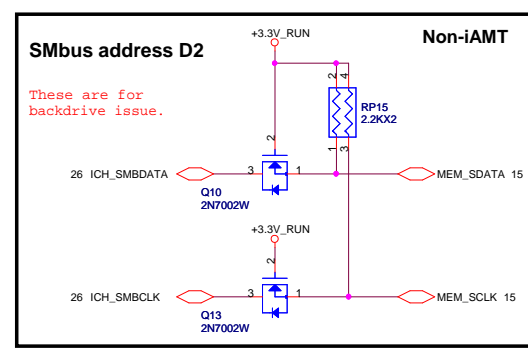
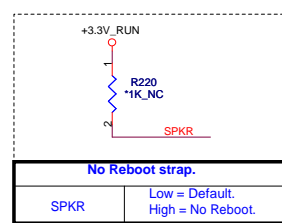
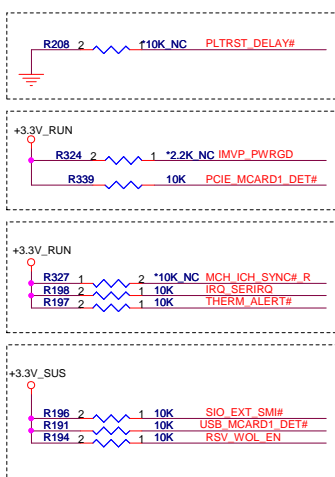
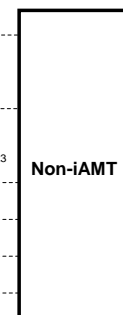
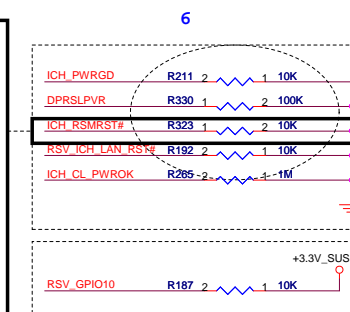
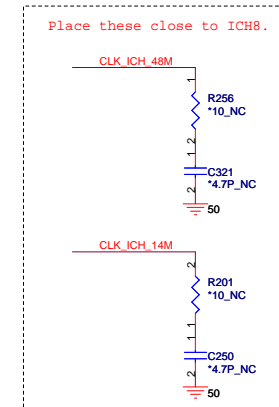
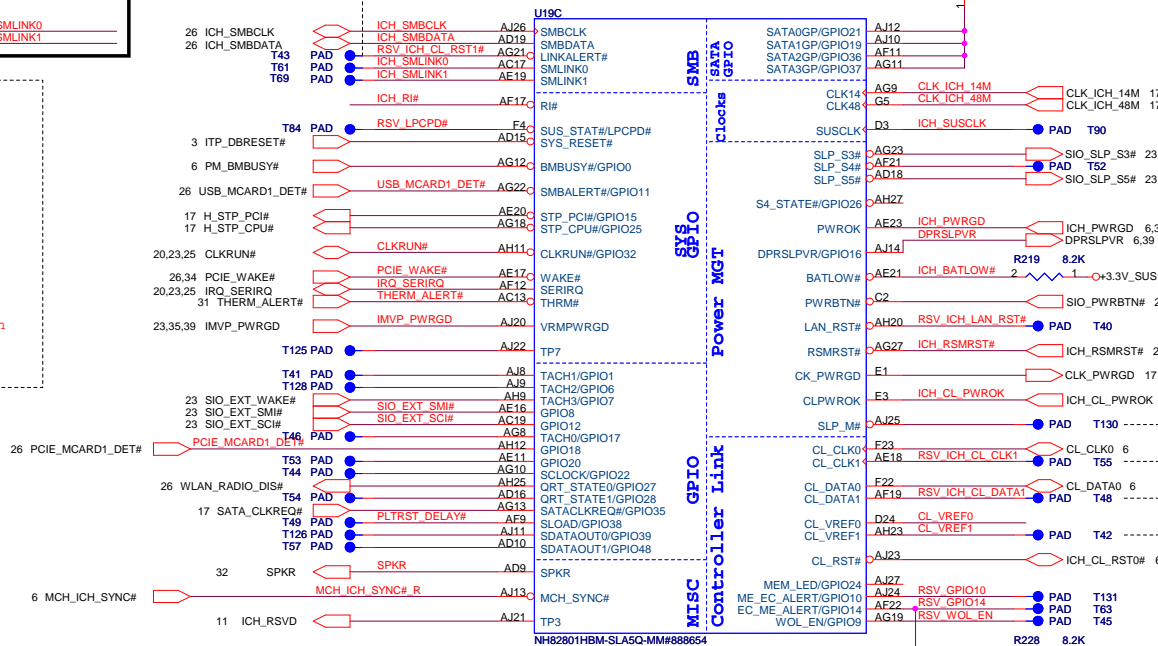
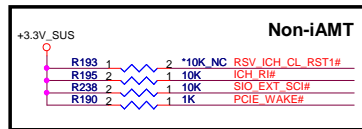
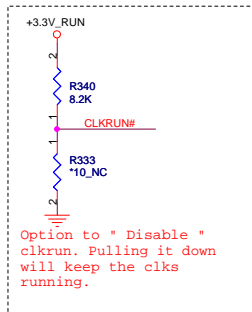
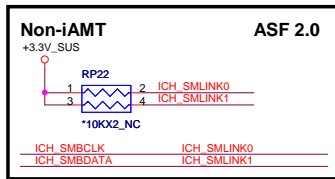
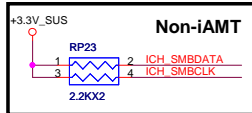
Size: Document Number VM9/VM8

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Rev 1A





QUANTA COMPUTER

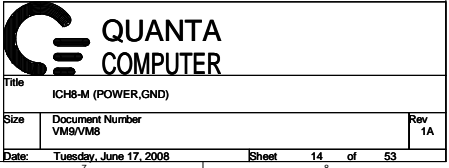
Title: ICH8-M (PM,GPIO,SMB,CL)

Size: Document Number VM9/VM8

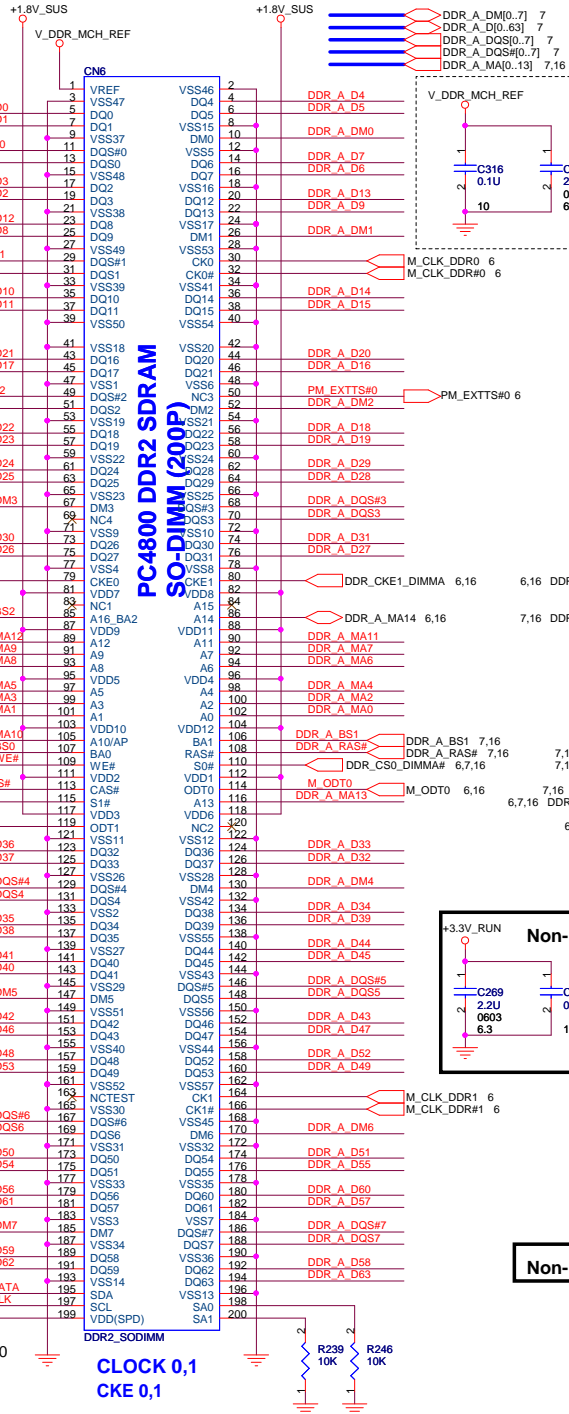
Date: Saturday, June 21, 2008

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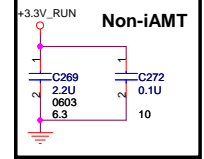


A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.

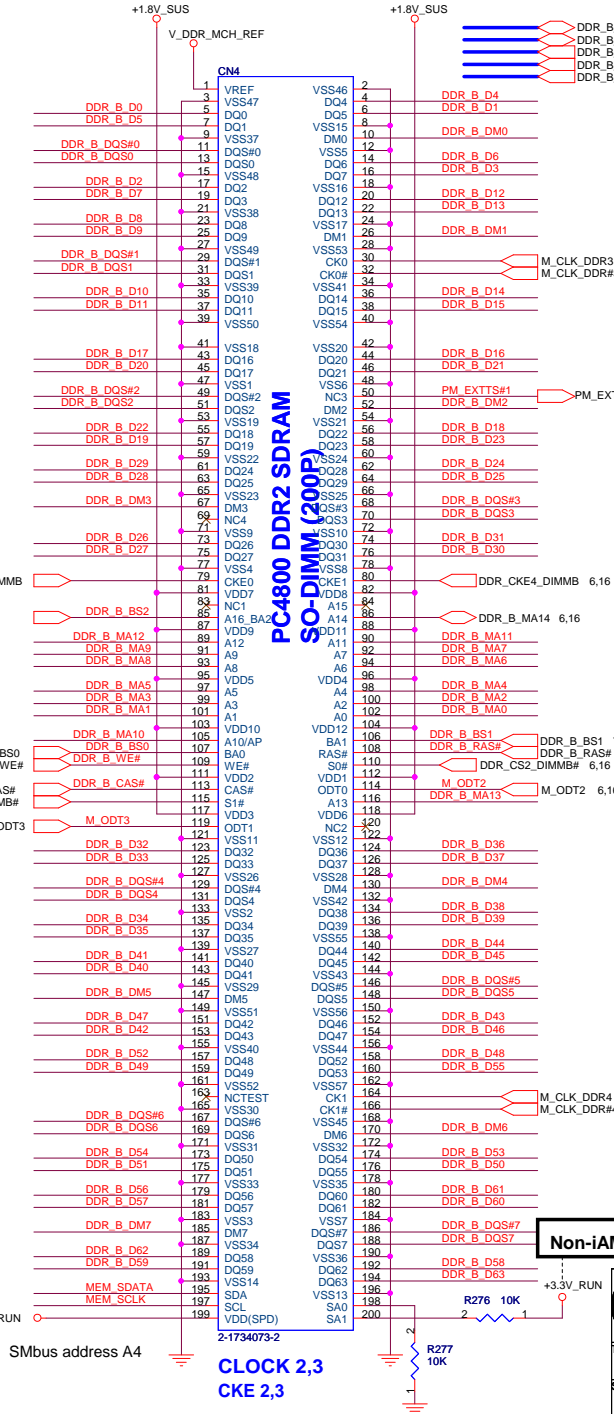


Non-iAMT

CLOCK 0,1
CKE 0,1

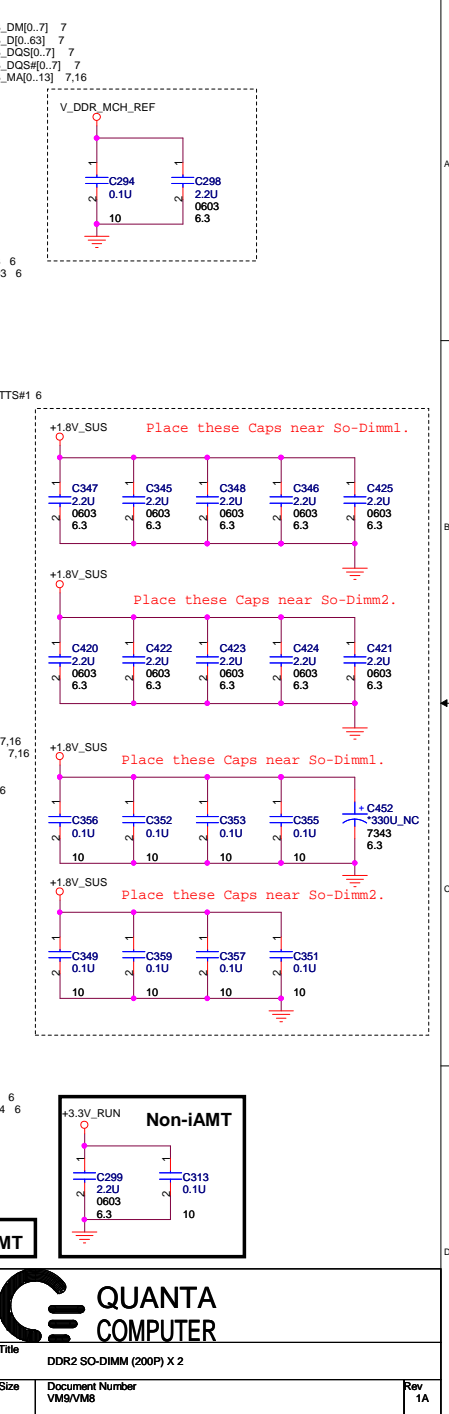


Non-iAMT

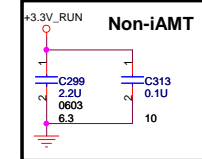


Non-iAMT

CLOCK 2,3
CKE 2,3



Non-iAMT

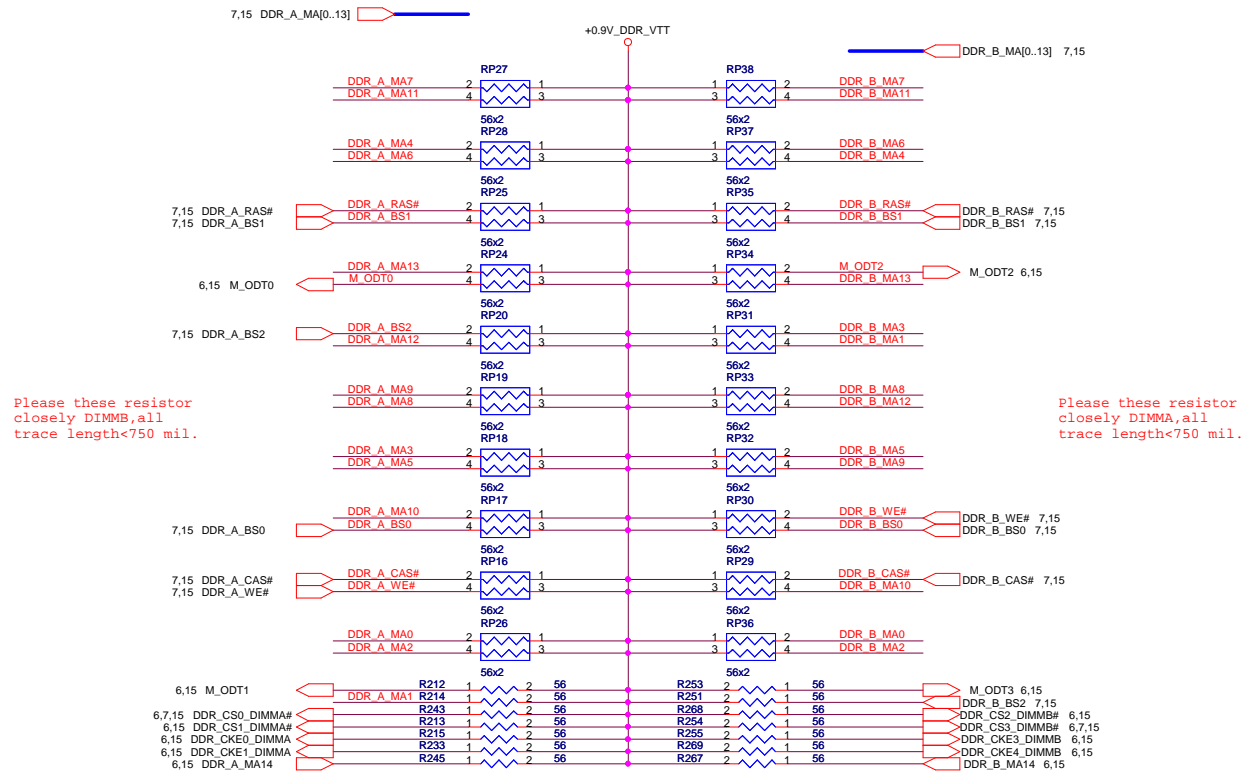
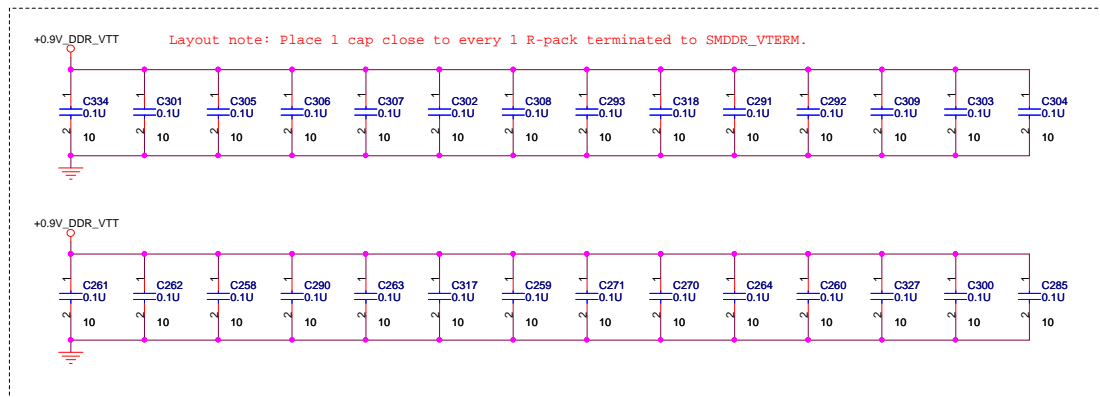



QUANTA COMPUTER

Title: DDR2 SO-DIMM (200P) X 2

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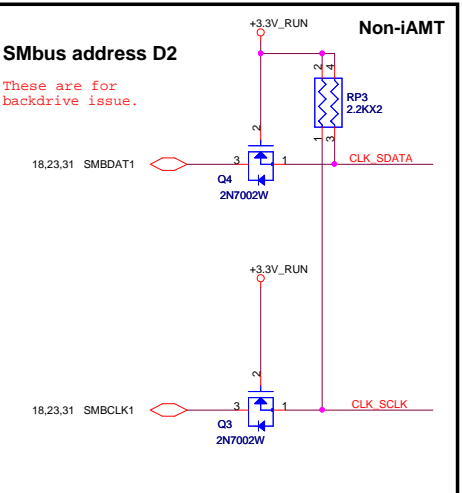
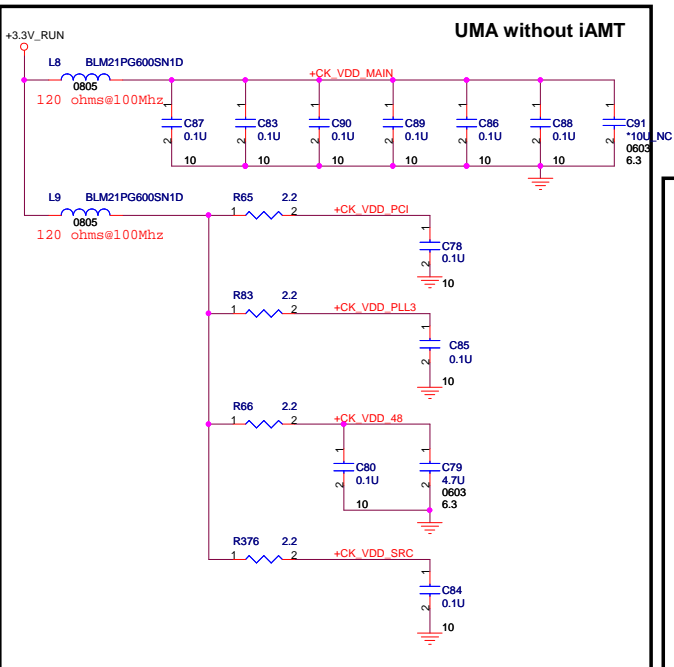
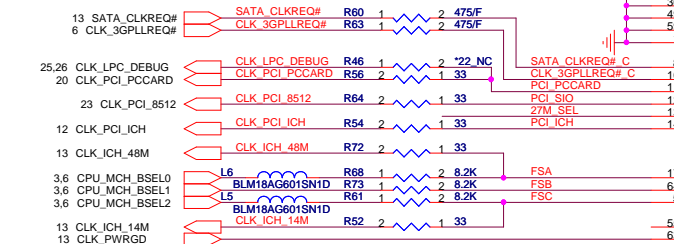
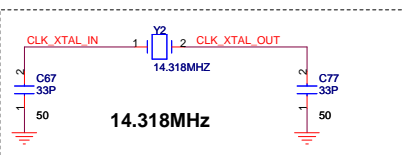
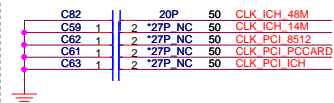


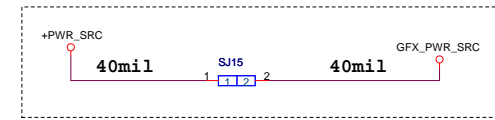
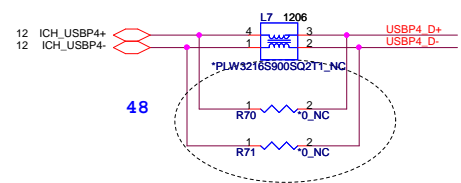
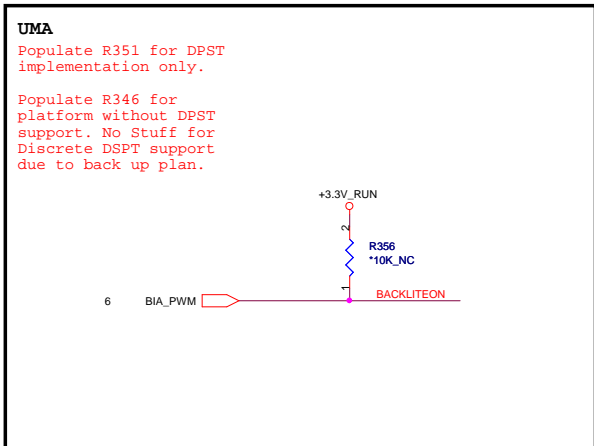
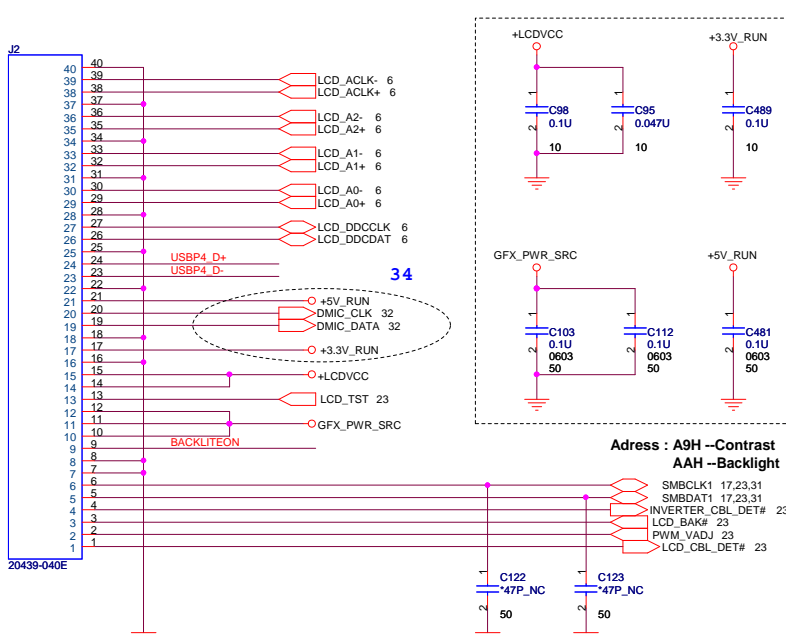
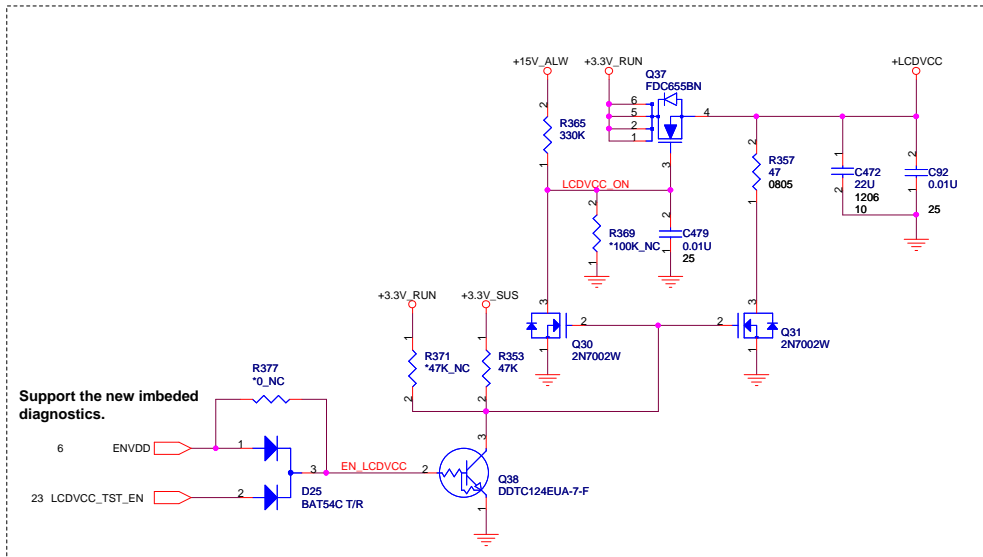
QUANTA

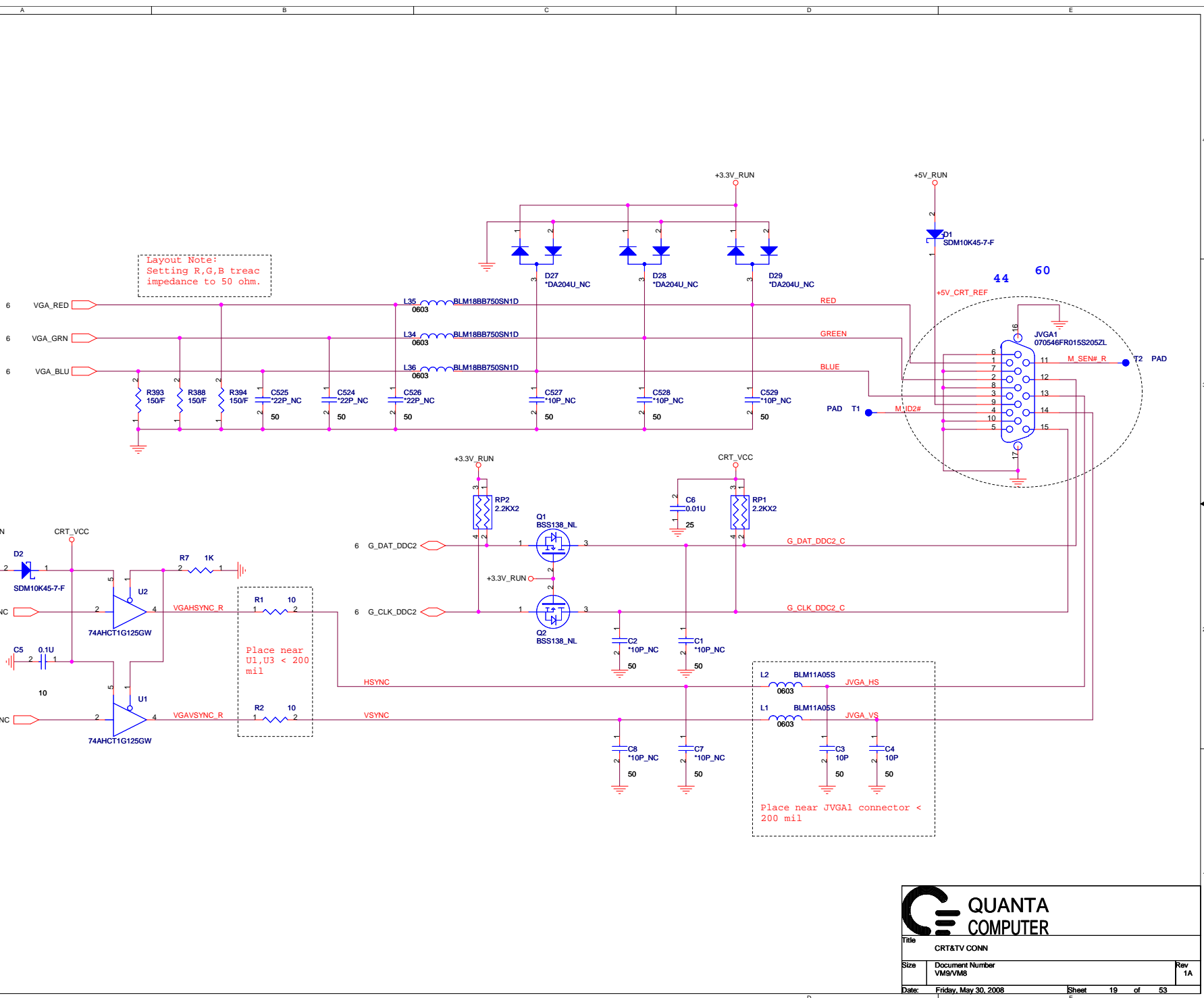
COMPUTER


Title DDR2 RES ARRAY		
Size	Document Number VM9/VM8	Rev 1A
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Add capacitor pads for improving WWAN.



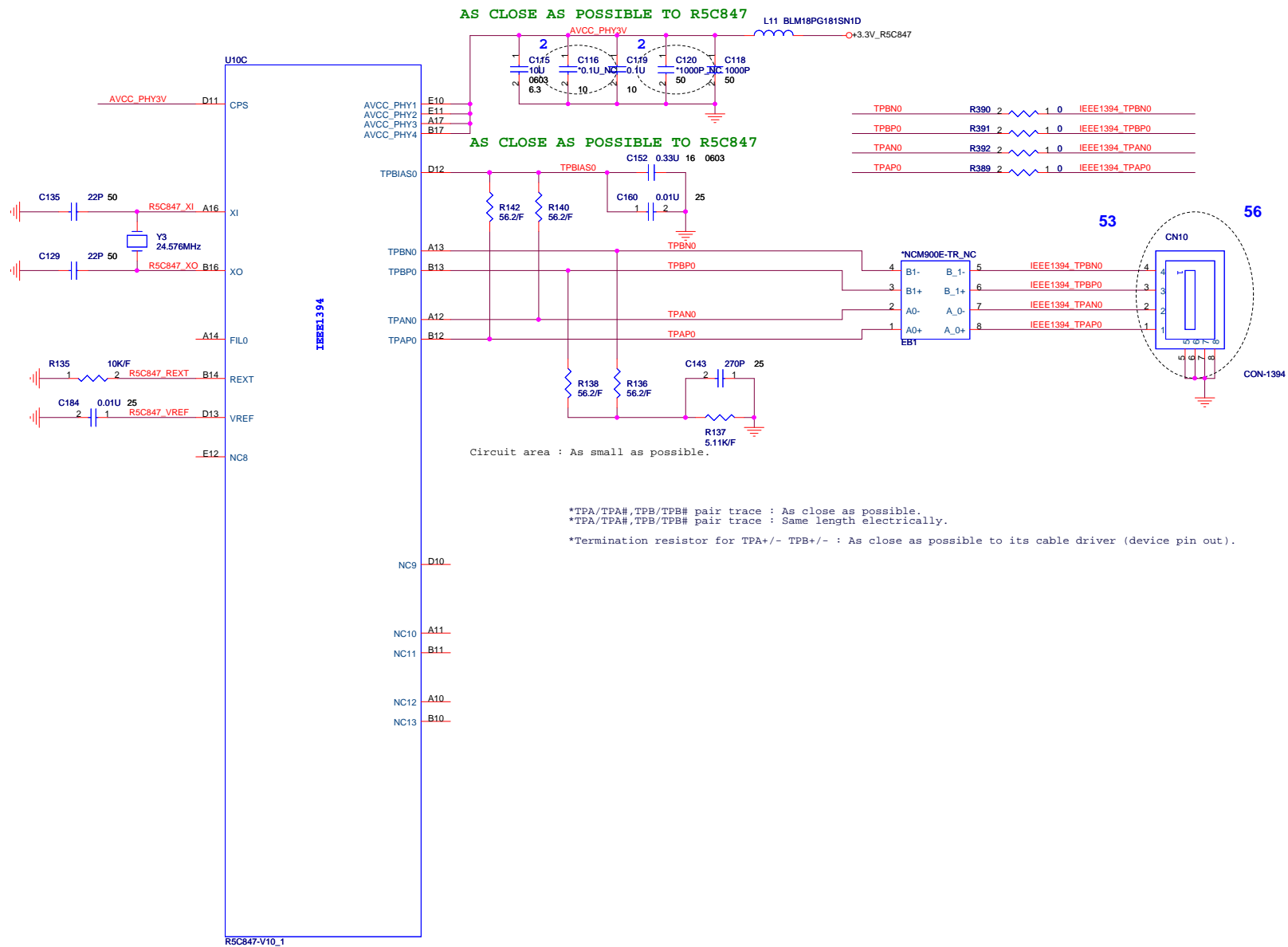


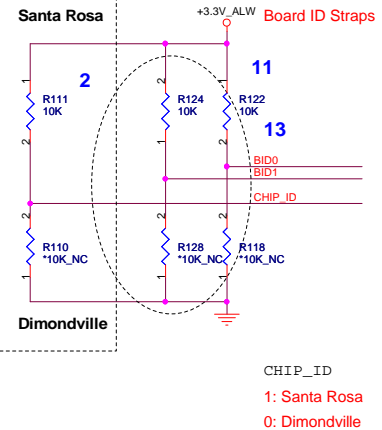
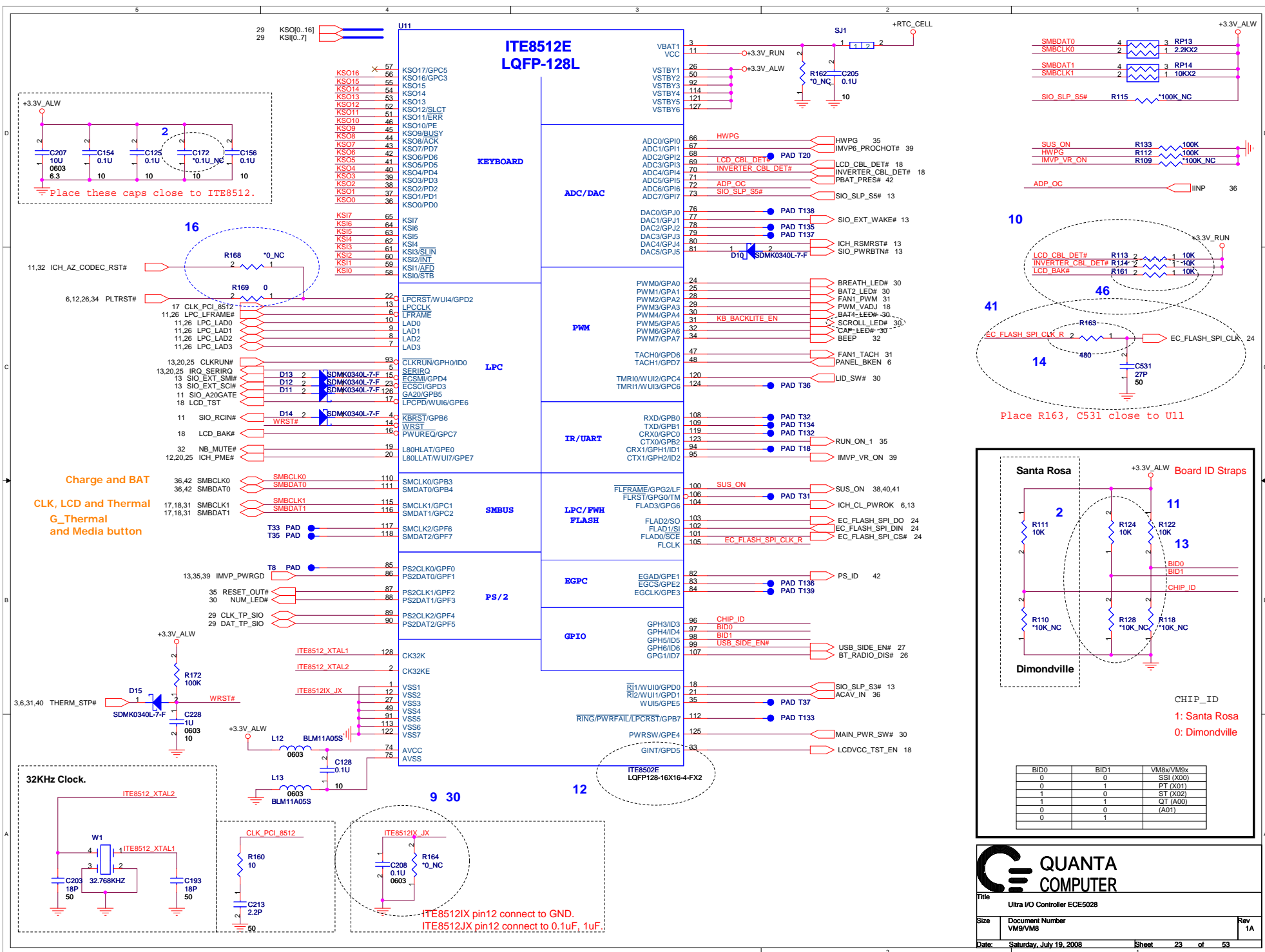




QUANTA
COMPUTER

Title CRT&TV CONN		
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BID0	BID1	VM8x/VM9x
0	0	SSI (X00)
0	1	PT (X01)
1	0	ST (X02)
1	1	OT (A00)
0	0	(A01)
0	1	

Title: Ultra I/O Controller ECE5028

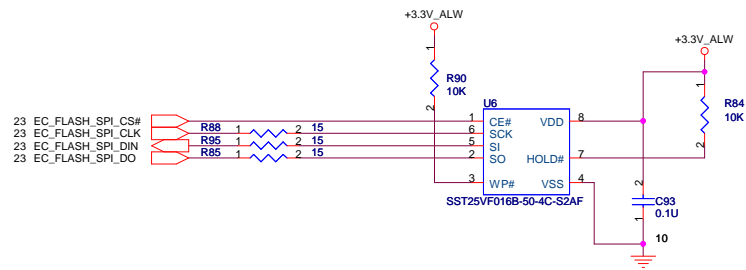
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Date: Saturday, July 19, 2008

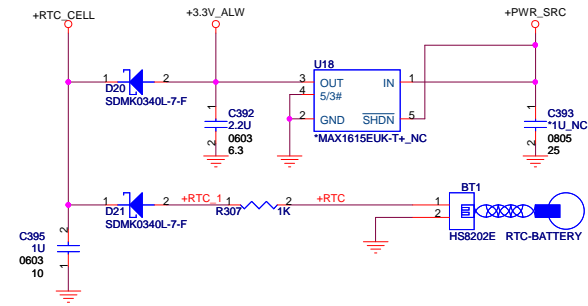
Sheet: 23 of 53

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16Mbit (2M Byte), SPI



RTC BATTERY



Ultra I/O Controller ECE5028

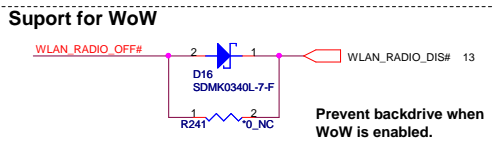
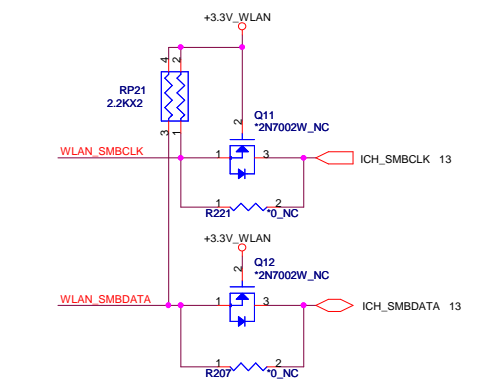
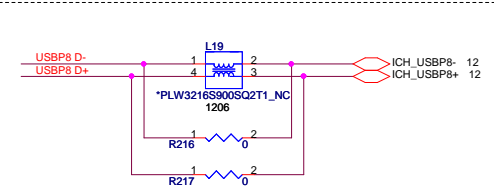
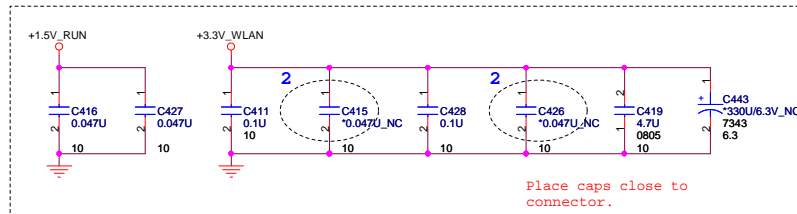
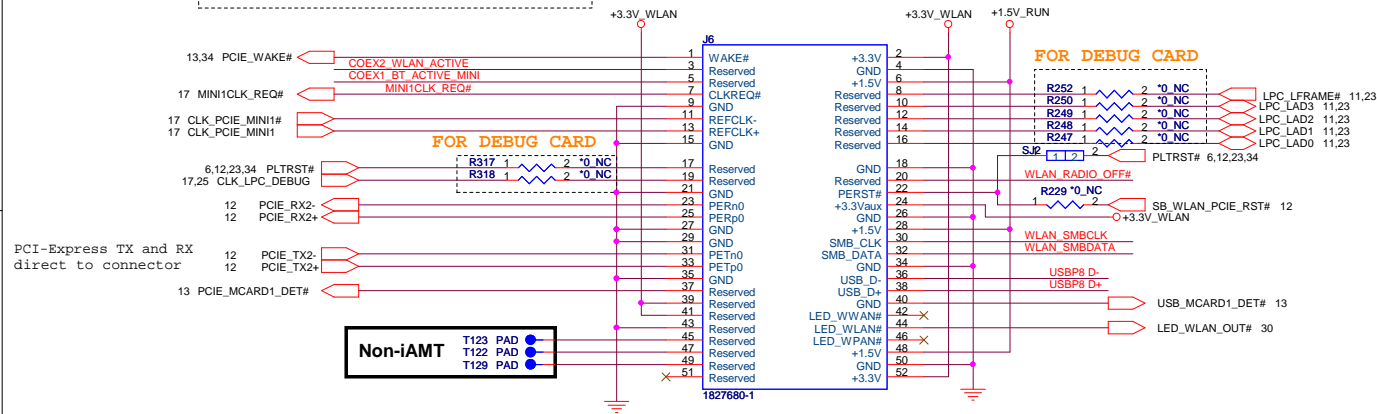
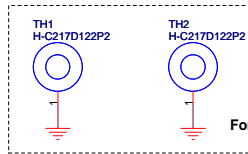
Size Document Number
VM9/VM8

Date: Friday, May 30, 2008

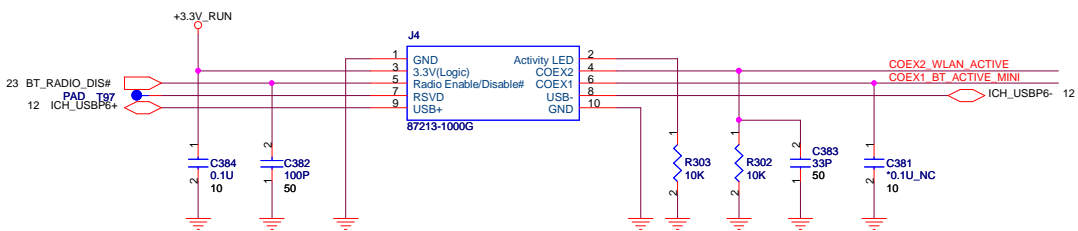
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1A

MiniCard WLAN connector

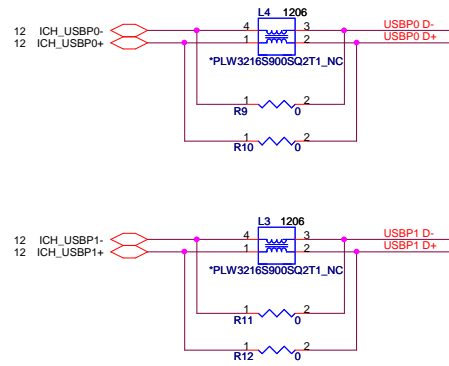


Bluetooth

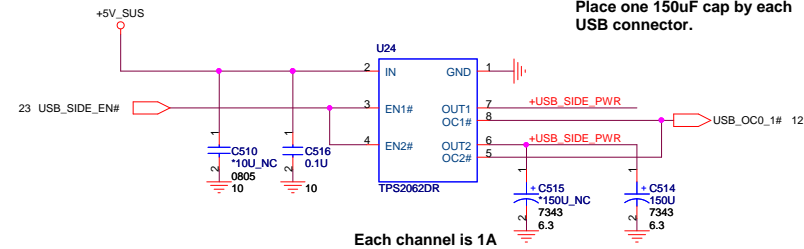
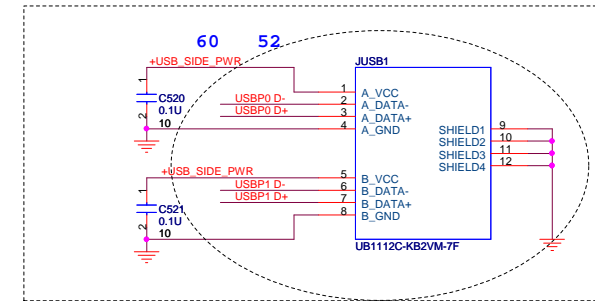


Title			MDC CONN.
Size	Document Number	Rev	
	VM9/VM8	1A	
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External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



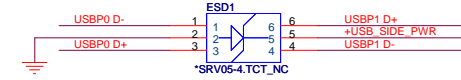
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



Place one 150uF cap by each USB connector.

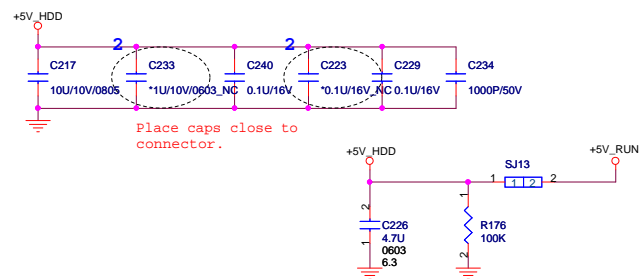
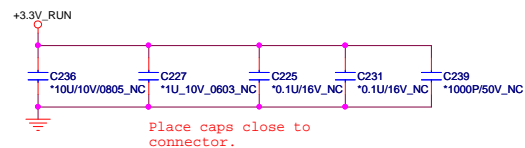
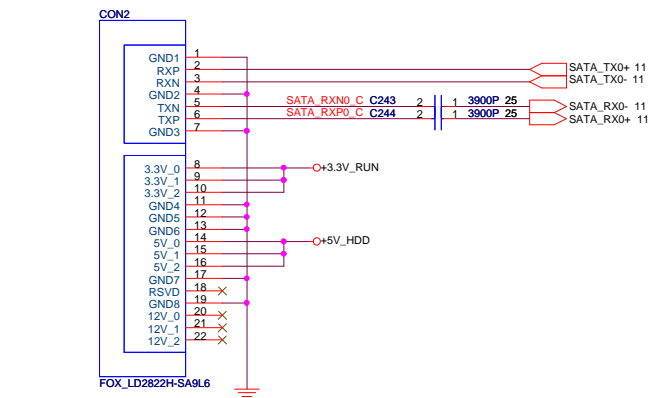
Each channel is 1A

Place ESD diodes as close as USB connector.



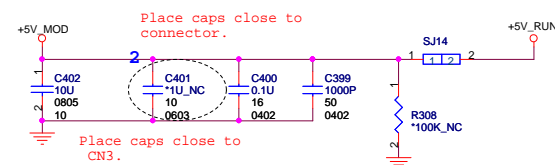
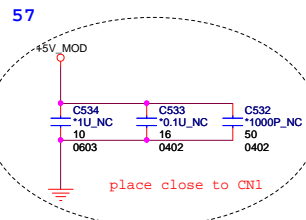
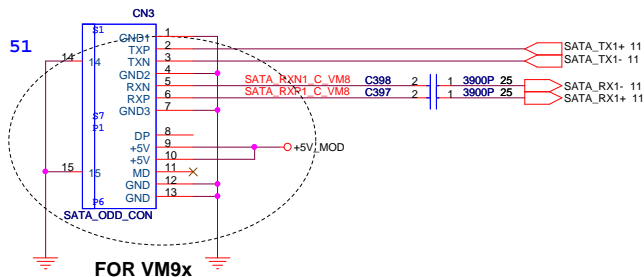
Title			SERIAL PORT & USB
Size	Document Number	Rev	
	VM9/VM8	1A	
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SATA HDD Connector.



SATA ODD Connector.

FOR VM8x



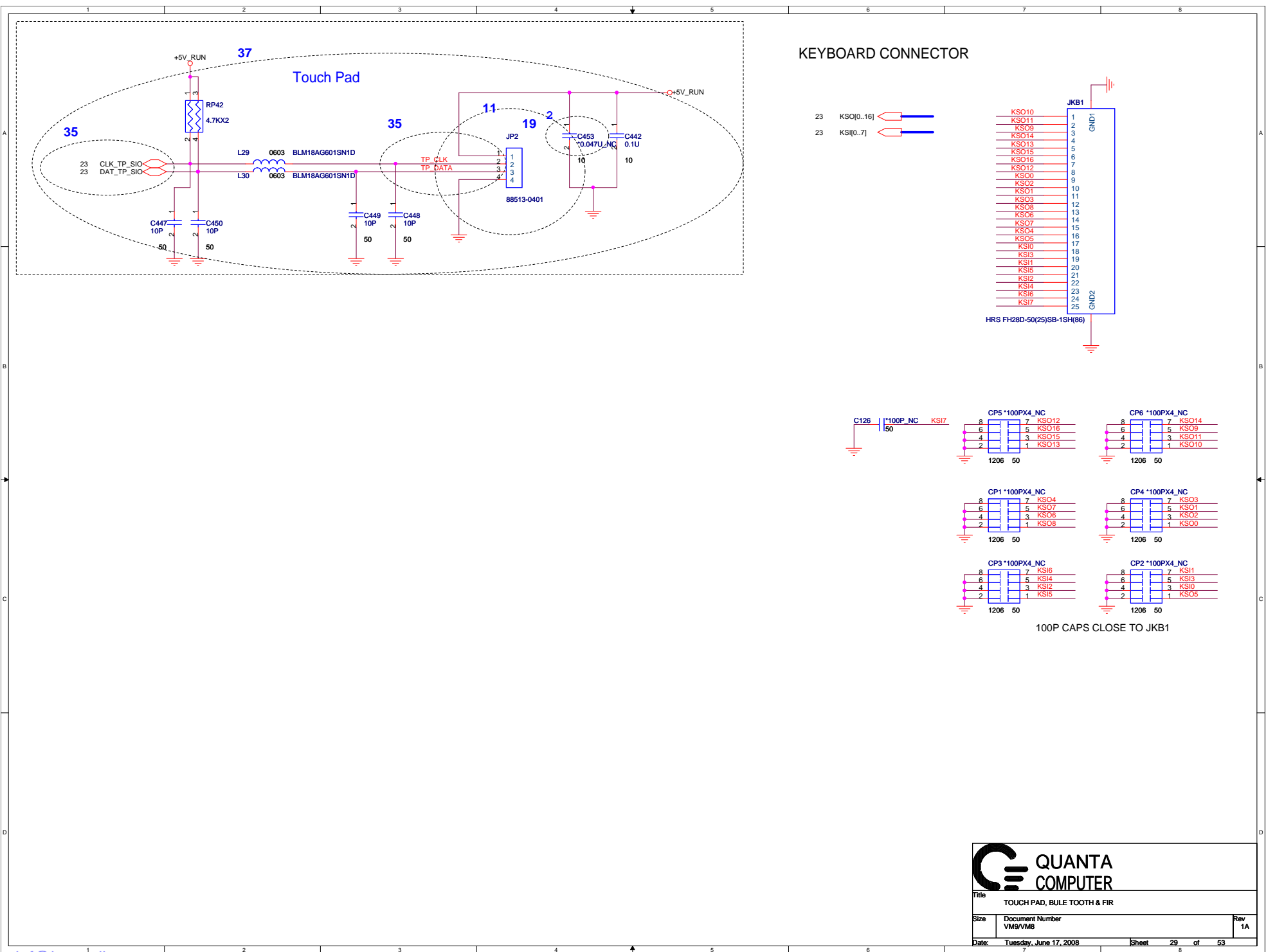
Title SATA (HDD&CD_ROM)

Size Document Number VM9/VM8

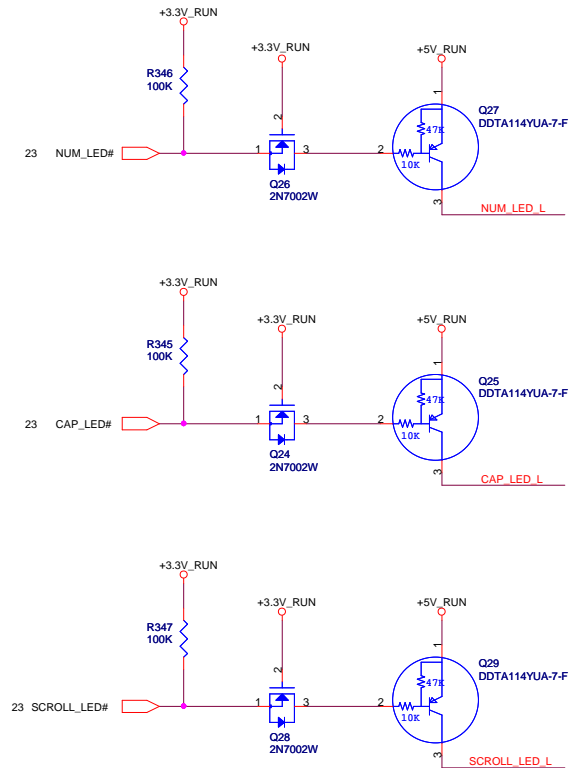
Date: Tuesday, June 17, 2008

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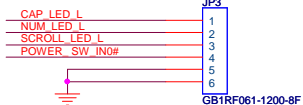


Keyboard LED

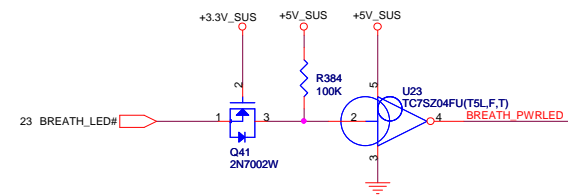


Dash board connector

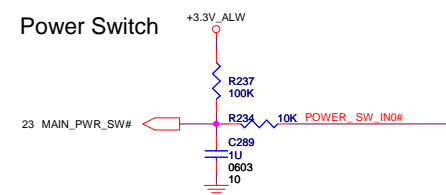
20



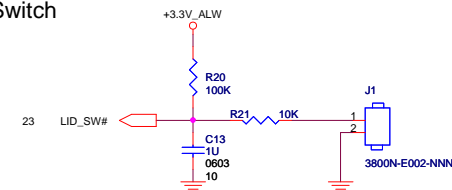
Power & Suspend.



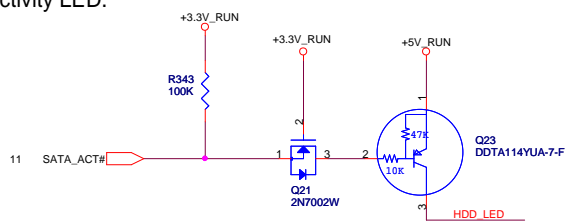
Power Switch



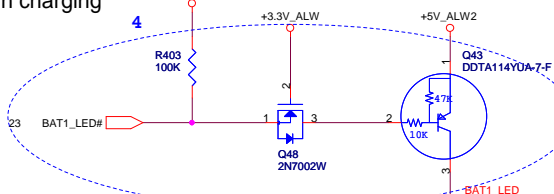
LID Switch



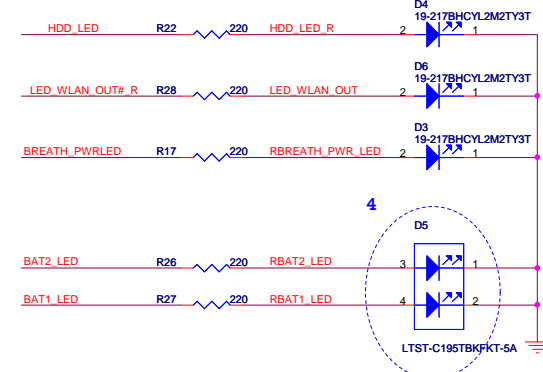
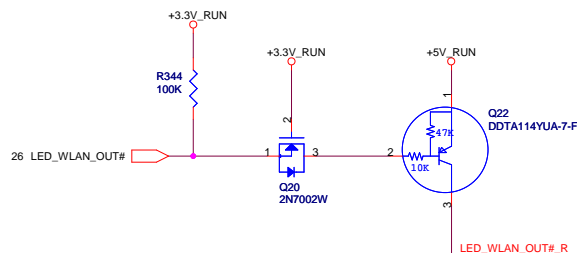
HDD activity LED.



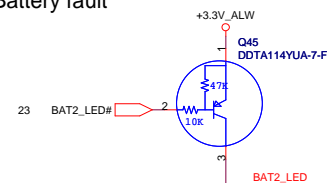
Battery in charging



WLAN



Battery fault



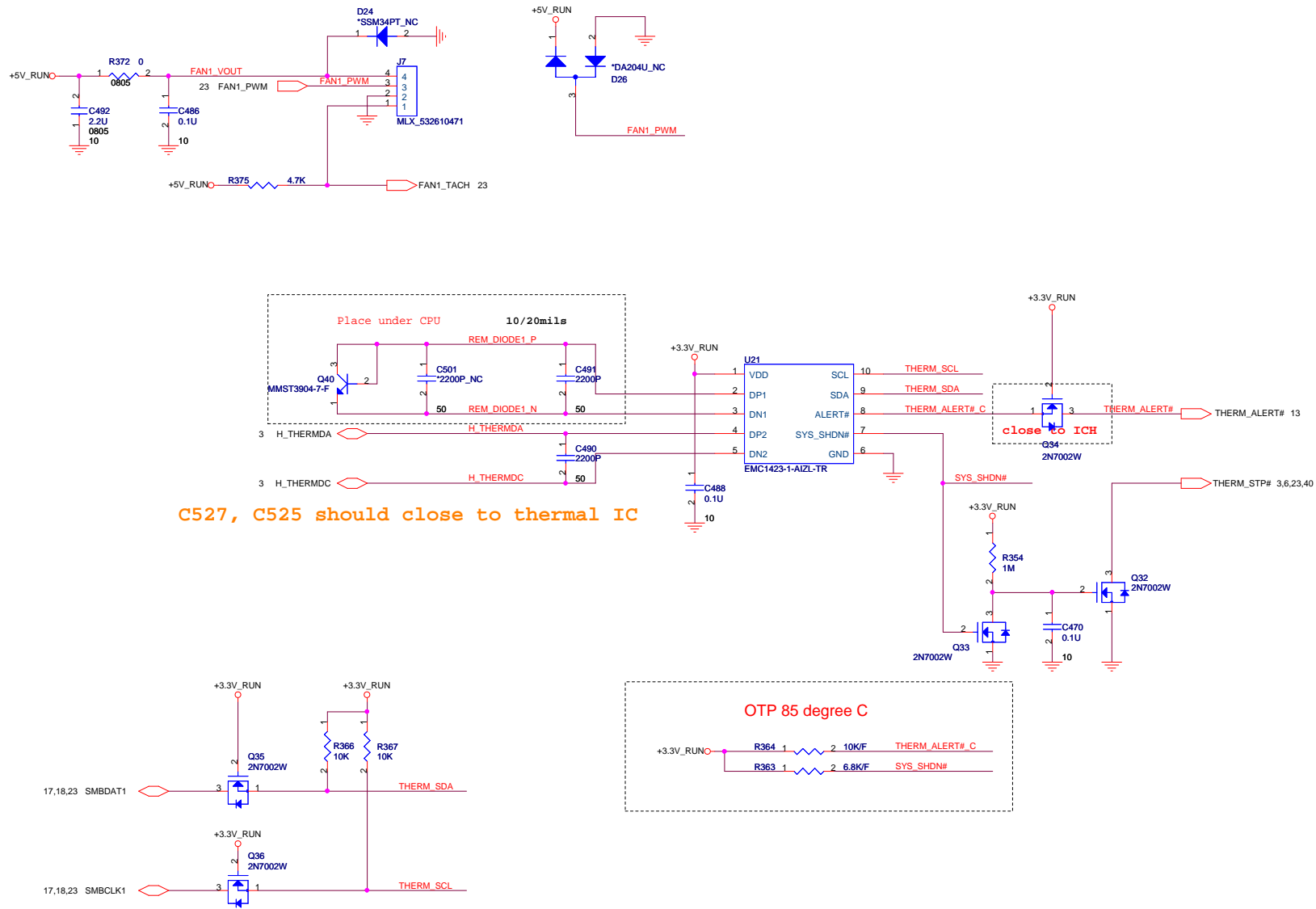
Title SWITCH, KEYBOARD & LED

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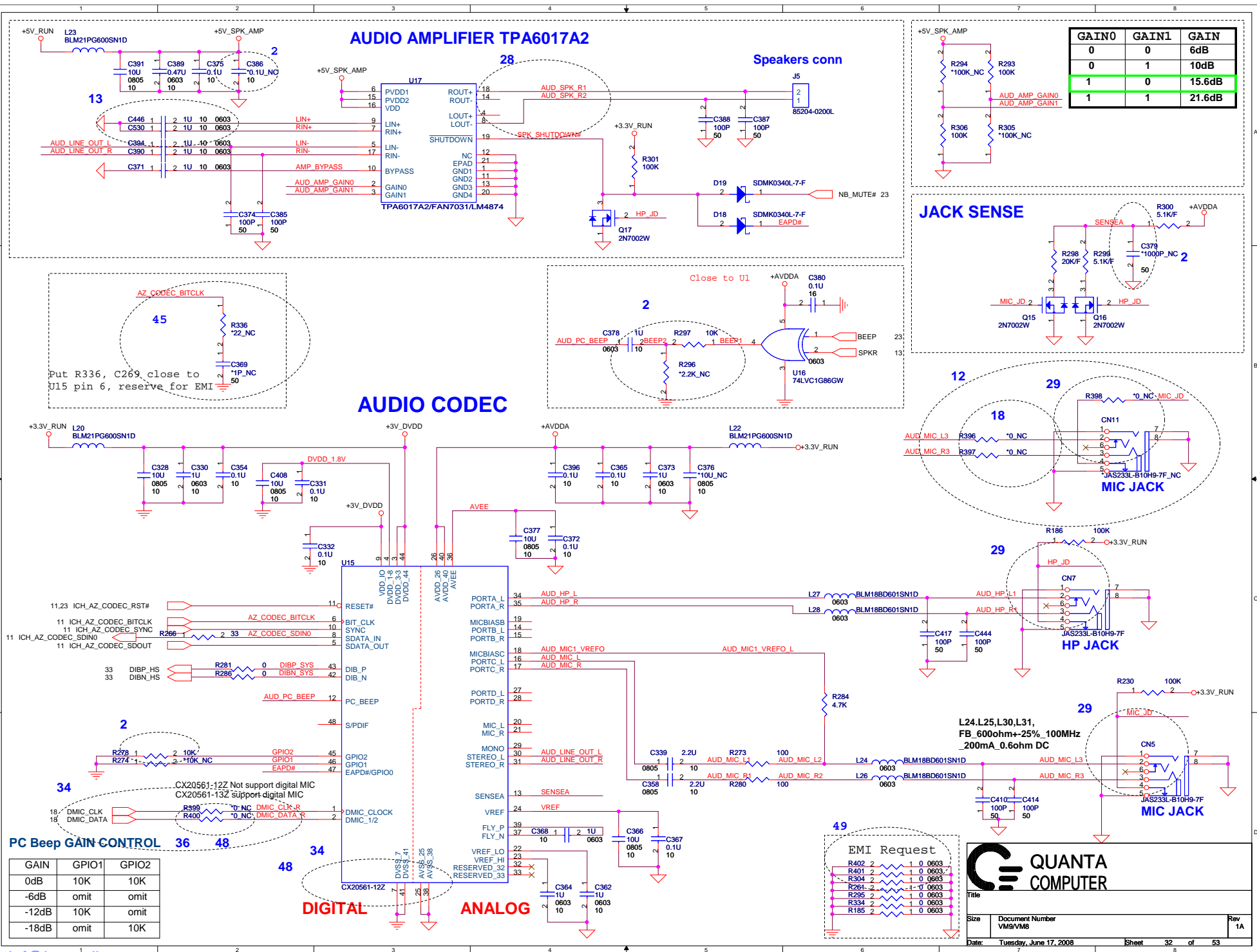
Title FAN & THERMAL

Size Document Number VM9/VM8

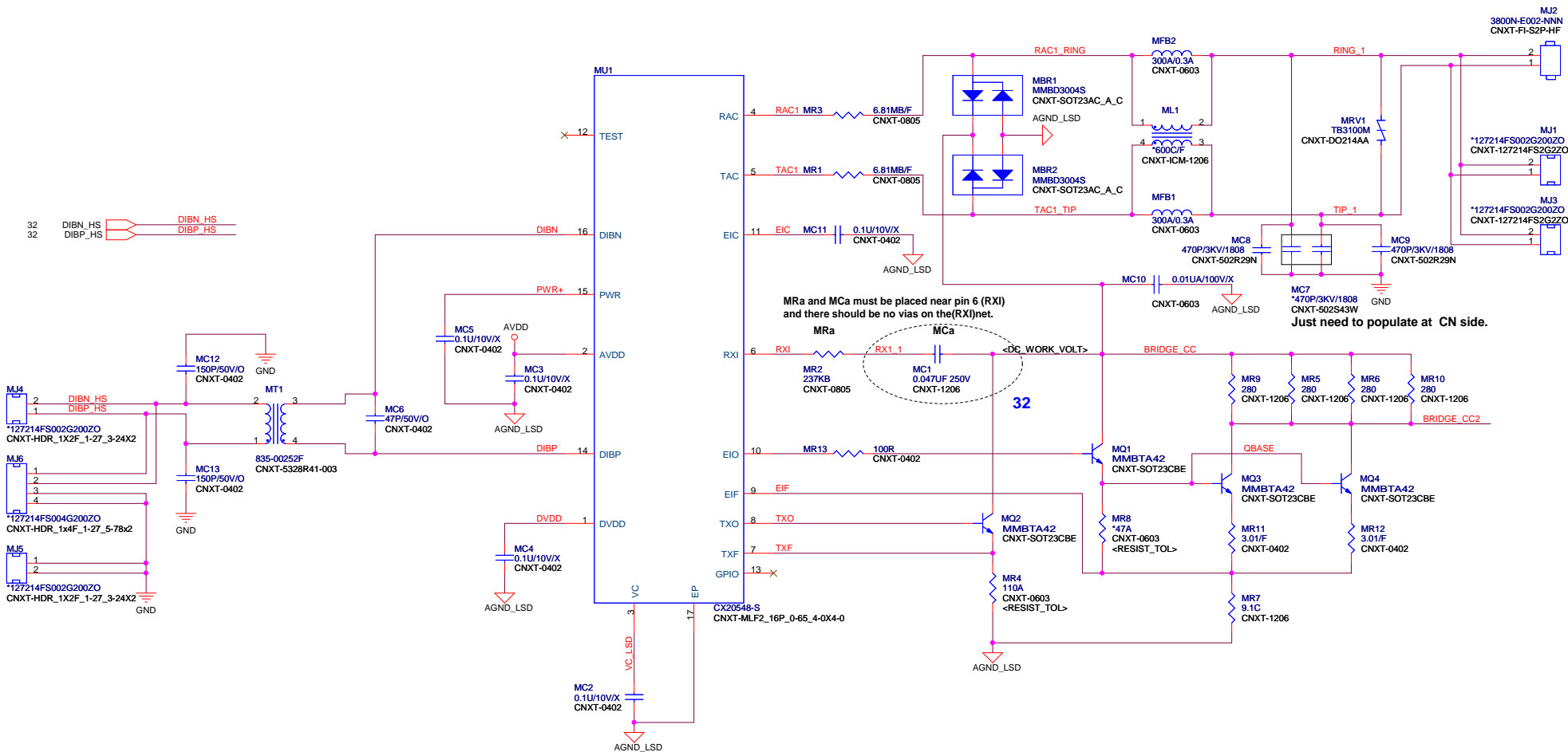
Date: Friday, May 30, 2008


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Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005
4		

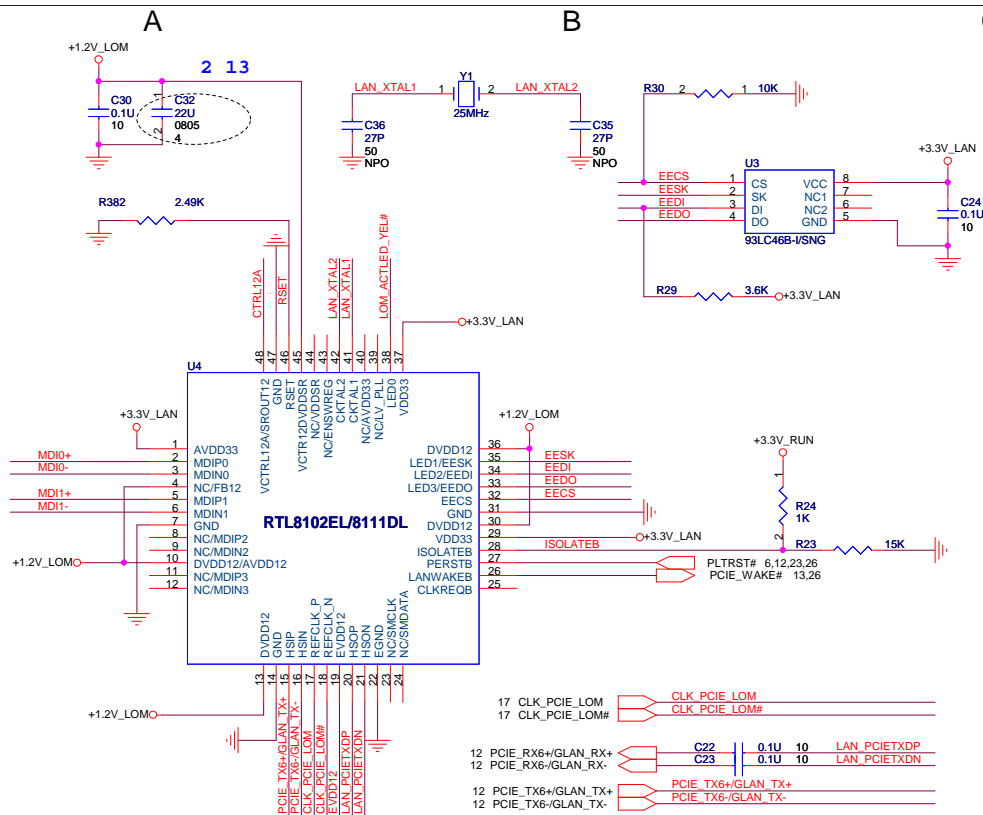




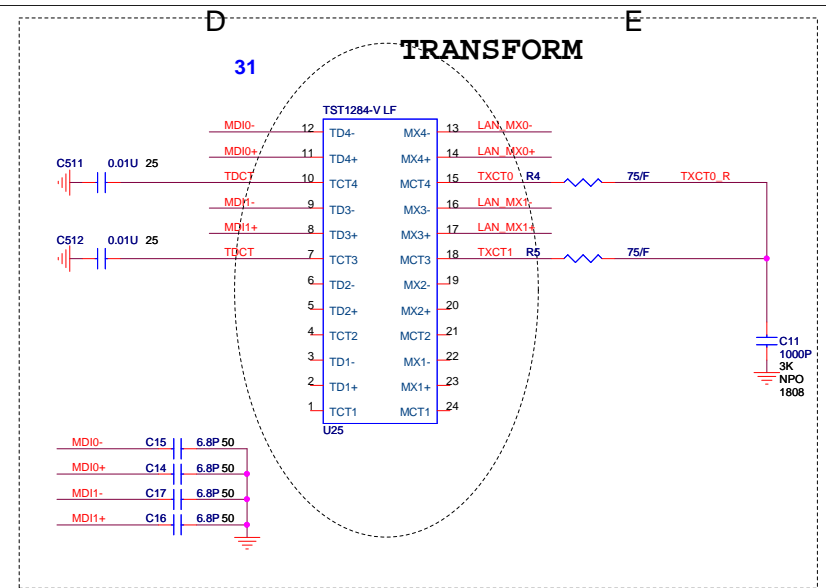
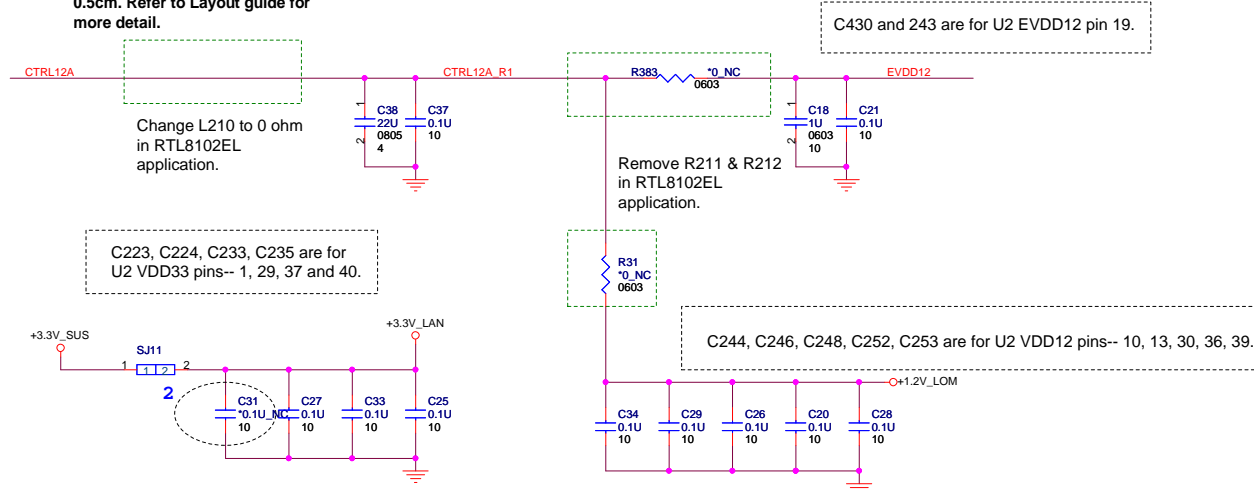
QUANTA

COMPUTER

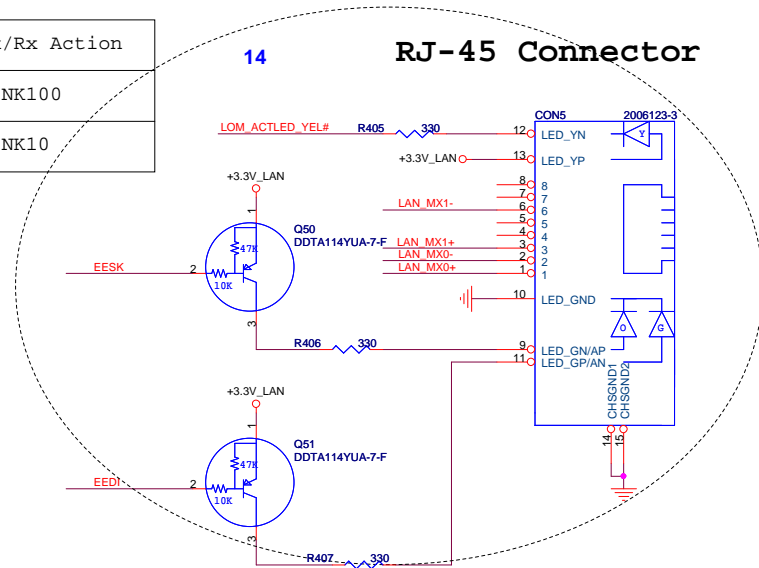
Title		Rev 1A
Size	Document Number VM9/VM8	
Date: Friday, May 30, 2008	Sheet 33 of 53	

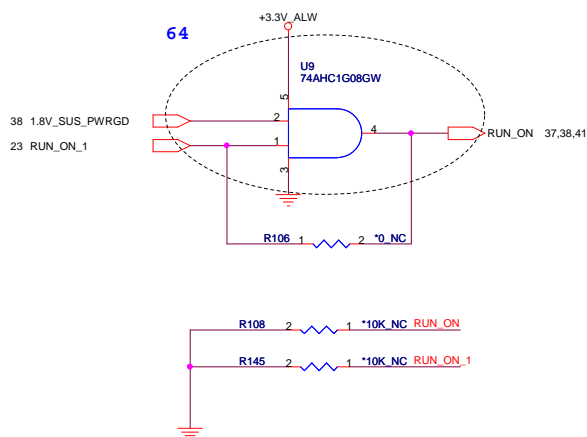
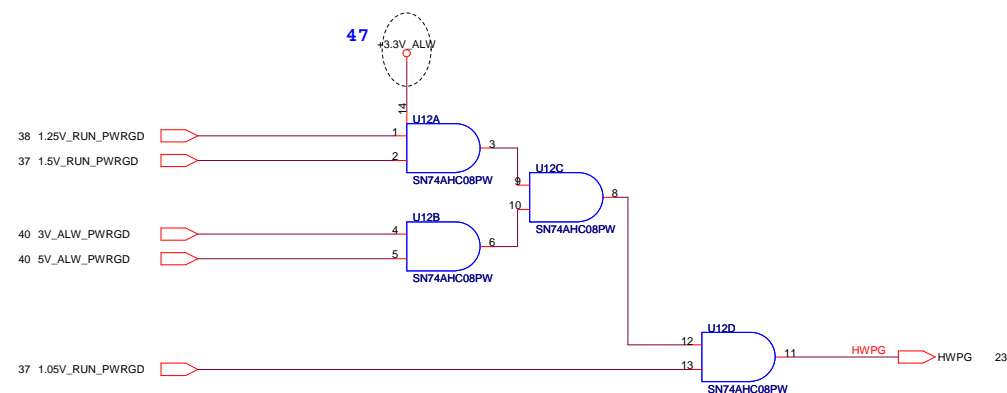
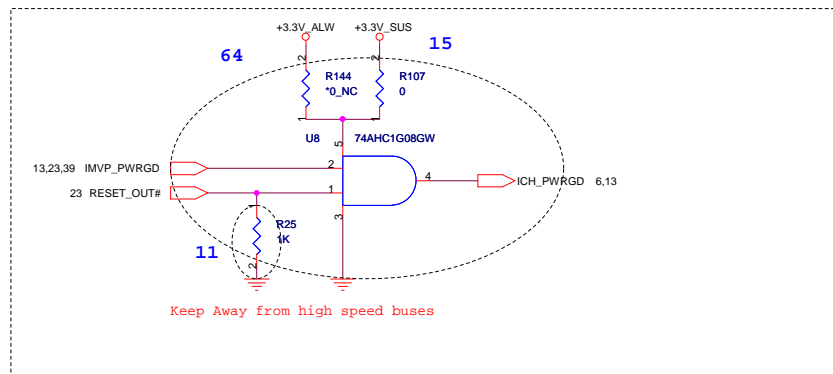


Note 1: The Trace length between L210 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L210 must be within 0.5cm. Refer to Layout guide for more detail.



LED0	Tx/Rx Action
LED1/EESK	LINK100
LED2/EEDI	LINK10





Title System Reset Circuit

Size Document Number VM9/VM8

Date: Friday, July 25, 2008

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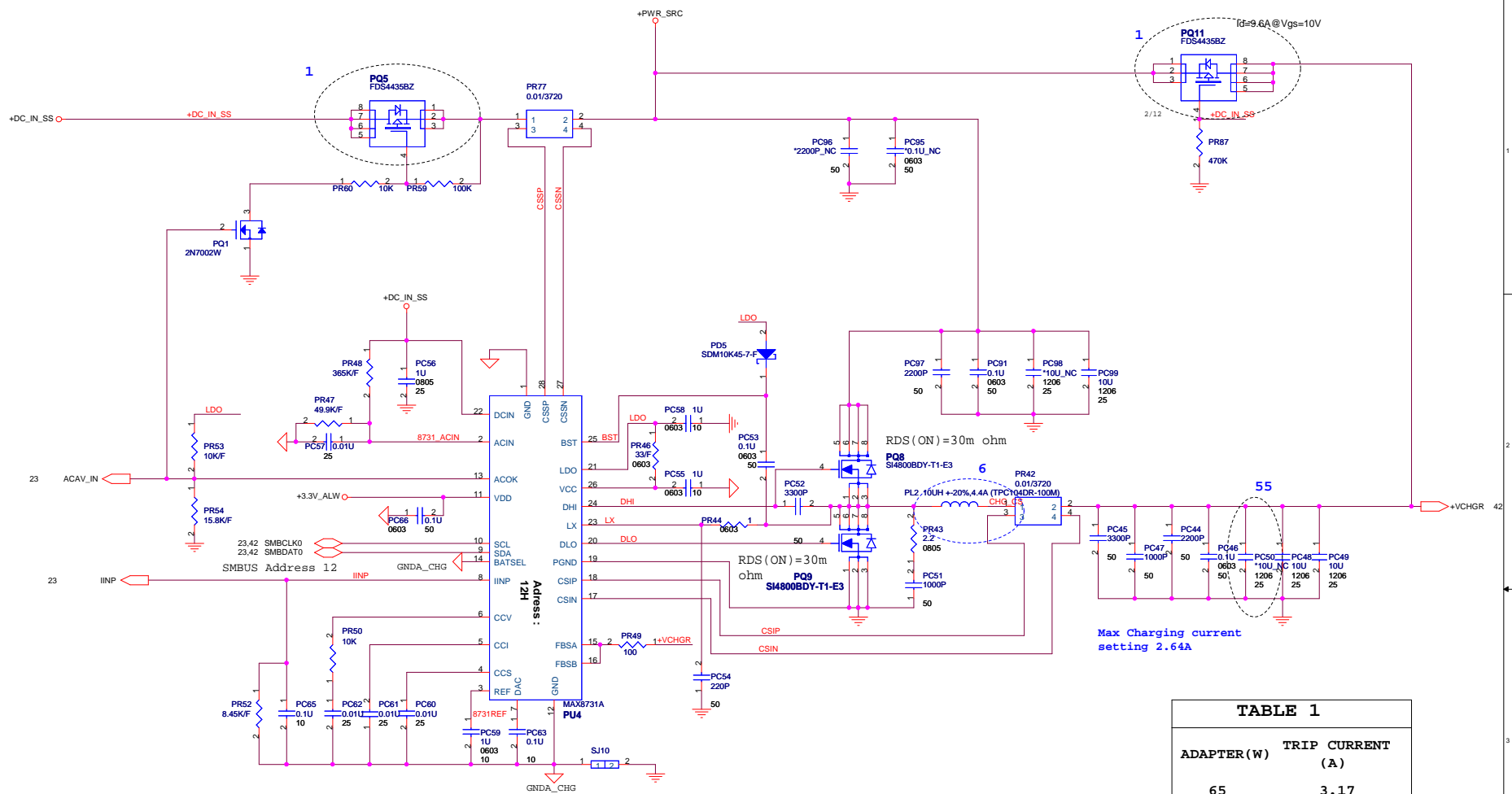


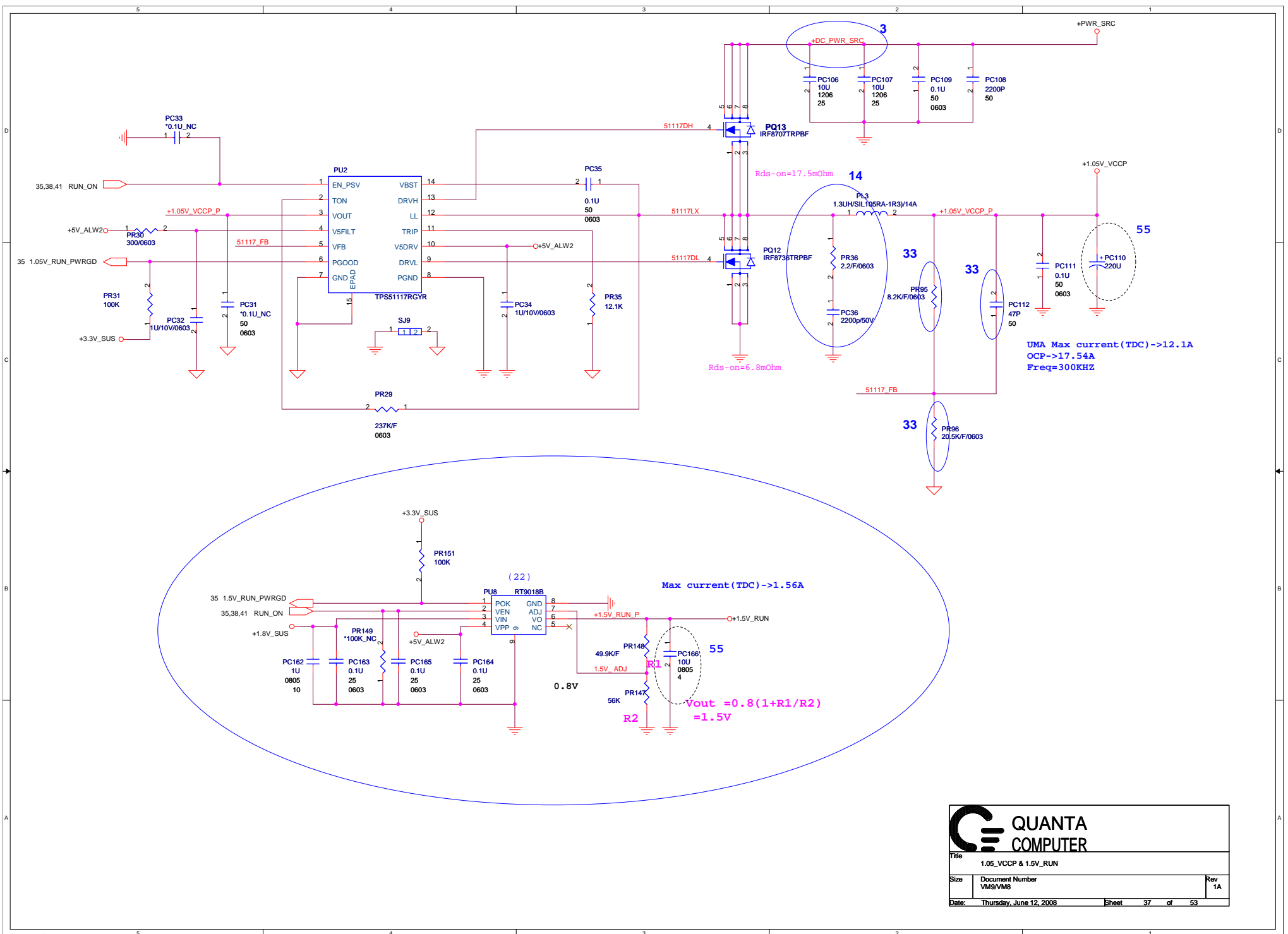
TABLE 1	
ADAPTER (W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.26 (see note3)

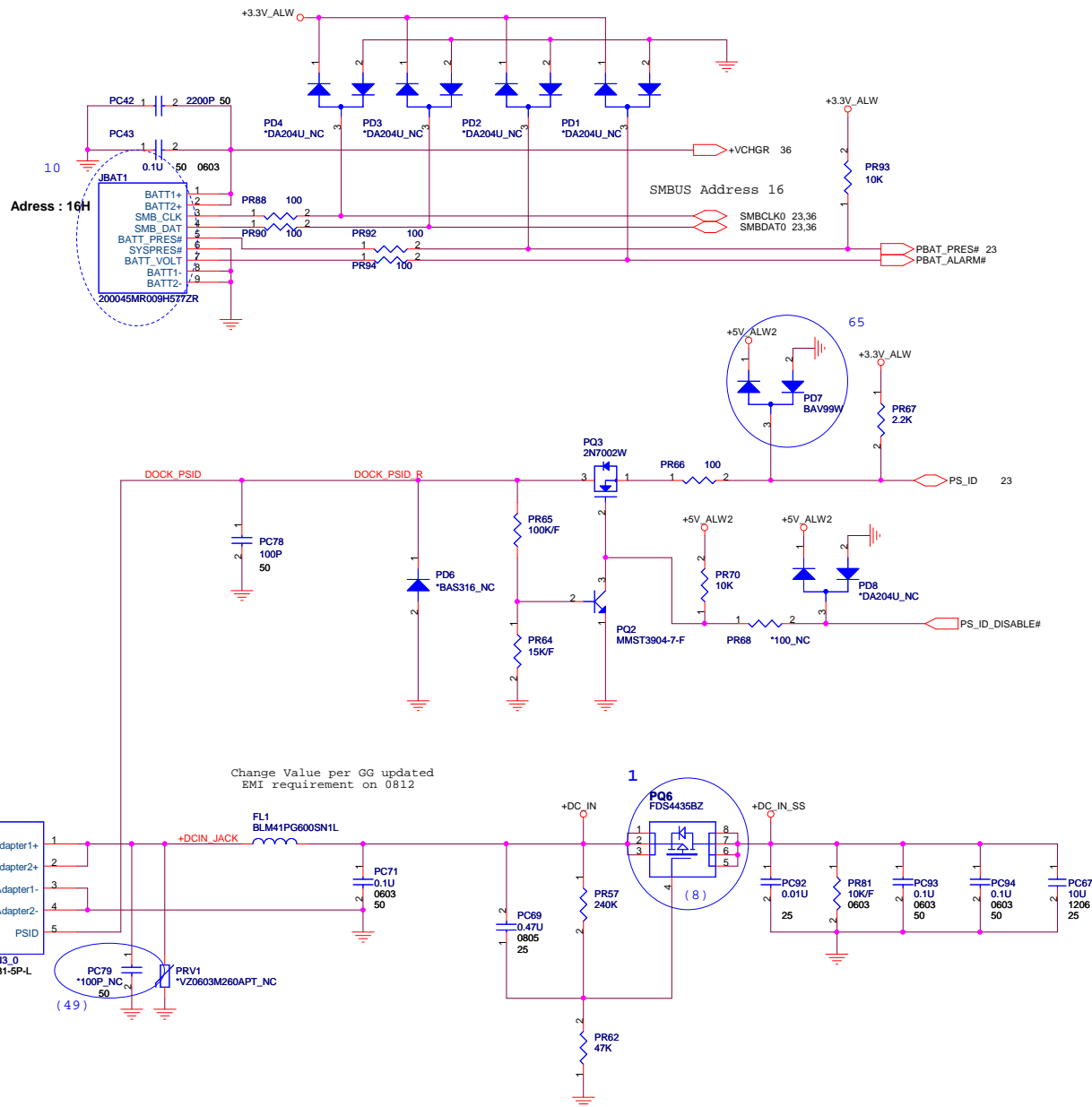
QUANTA
COMPUTER

File: Charger (SL88731)

Size: Document Number VMA/VM8 Rev 1A

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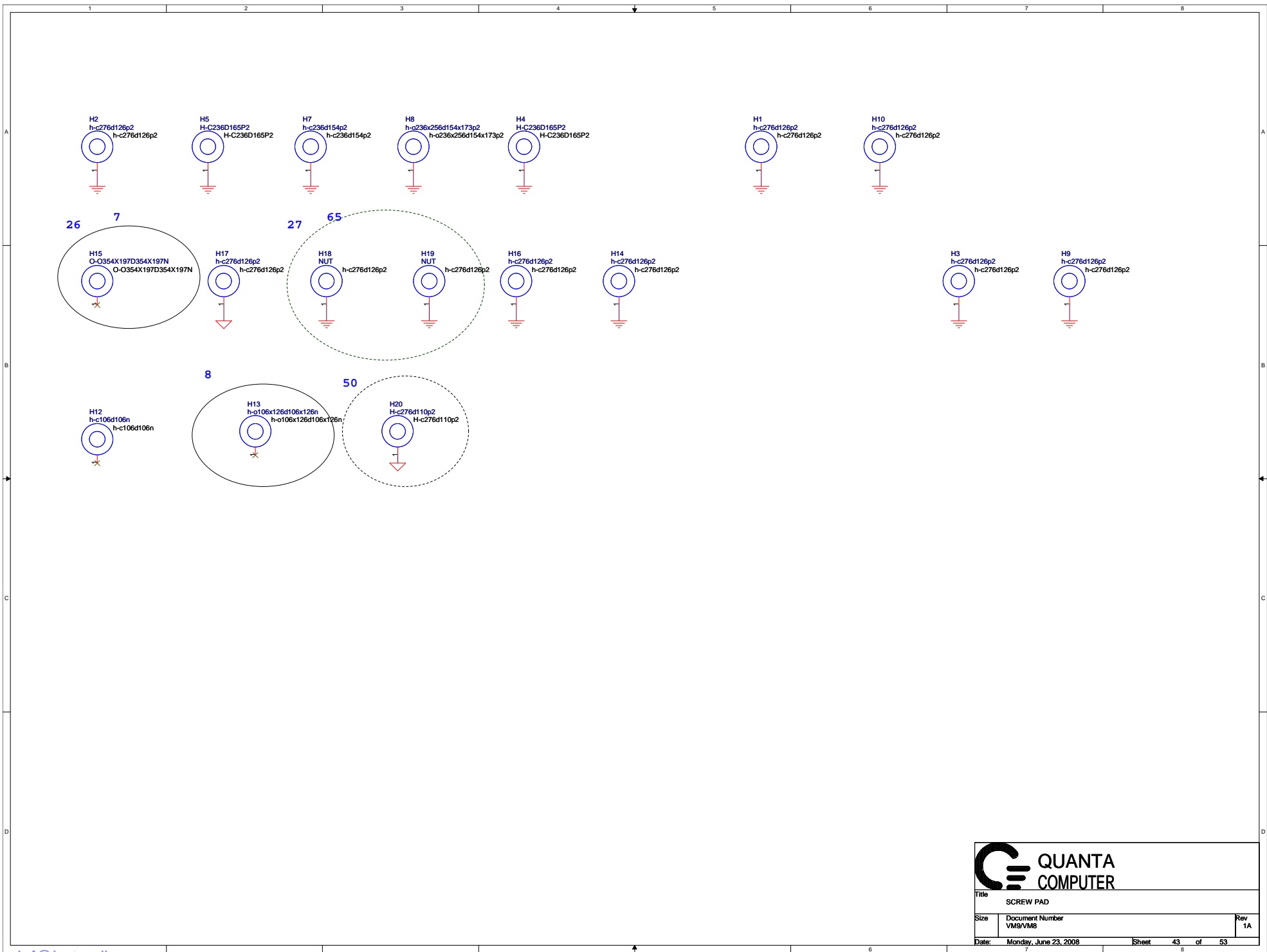



Title
DCIN, BATT CONNECTOR

Size
Document Number
VM9/VM8

Rev
1A

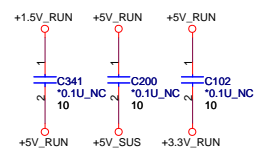
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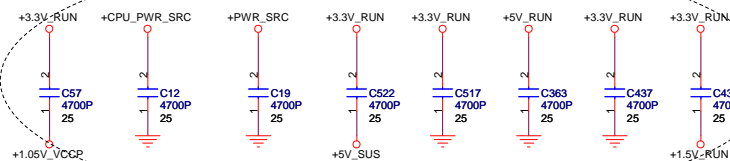
		QUANTA COMPUTER	
Title: SCREW PAD			
Size:	Document Number: VM9/VM8		Rev: 1A
Date:	Monday, June 23, 2008		Sheet: 43 of 53

Reserved for EMI.

Stitching caps for PCI bus.



40 Stitching caps for PCI EMC.



Title
EMI CAP

Size
Document Number
VM9/VM8

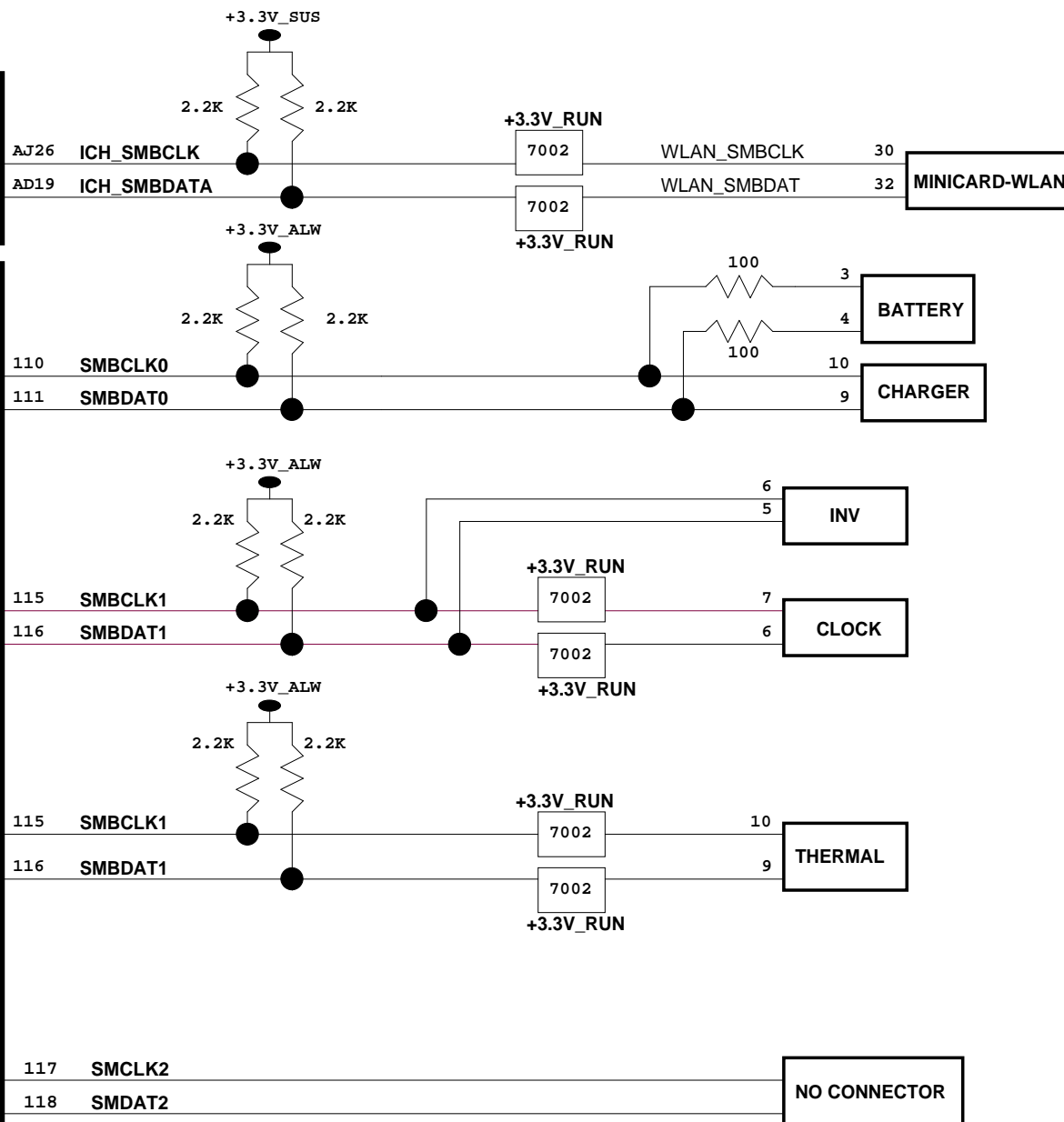
Date: Tuesday, May 27, 2008

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ICH8-M

**SIO
ITE8512**



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